



Features

- Ready to use DVB-S compliant modulator core
- For Virtex-5™, Virtex-4™ and Spartan™-3/E/A FPGAs.
 - Flexible input and symbol rates.
 - PCR restamping
 - Fully optimized single channel version.
 - Single clock (up to 125MHz+ for Spartan-3™, Virtex-4/5™)
 - Dynamically Programmable FEC 1/2, 2/3, 3/4, 5/6, 7/8.
 - Symbol rate from 1 to 31.25Msym/s
 - Dynamically programmable DUC
 - Full synthesizable RTL VHDL design (not delivered) for easy customization
 - Netlist version available for ISE 9.2 and later versions

Description

The MVD DVB-S core is a drop-in module that includes the following functions :

- Input data framer from Microprocessor, MPEG_ASI or MPEG_SPI source (MPEG_TS flow)
- modulator (Energy dispersal, Reed Solomon encoder, interleaver, FEC convolution encoder)
- Programmable RRC filter
- Flexible Digital Up Converter
- Modulator for IF output
- Output for simple DAC (14 bits) or complex DAC (2x16bits)

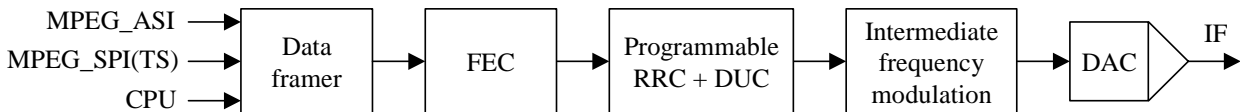
The MVD DVB-S core can be customized for specific application. In option, it can include :

- ASI interface core
- Ethernet UDP core for video on IP
- Direct 32 bit CPU interface for configuration parameters and MPEG_TS input flow

Applications

Low cost, fully integrated DVB-S compliant satellite transmitter modulator, from MPEG_TS to IF DAC.

Complete application fits into 3S500E and/or 3S700A depending on selected options.



Resource Utilization The core configuration may be set by conditional synthesis. Typical configuration with SPI (MPEG TS) input , CPU interface and complex DAC output.

	Slices	BRAMs	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation and testbench for simulation
Spartan3/E/A	4 400	6	16	2	
Virtex 4	4 600	6	15	2	
Virtex 5	2 600	4	15	2	

(values may vary depending on implementation options)

Ordering information and related cores

Parameters	Interfaces for MPEG_TS input stream	Designation
Fixed	SPI	MVD_DVBS_FIXED_SPI_NET
Fixed	ASI (1)	MVD_DVBS_FIXED_ASI_NET
GPIO programmable	SPI	MVD_DVBS_GPIO_SPI_NET
GPIO programmable	ASI (1)	MVD_DVBS_GPIO_ASI_NET
CPU programmable	SPI	MVD_DVBS_CPU_SPI_NET
CPU programmable	SPI + ASI (1) +CPU (2)	MVD_DVBS_CPU_SPI_ASI_CPU_NET

(1) ASI can be serial or parallel (please specify).

(2) CPU interfaces compatible with 8, 16 or 32-bit, big or little endian processors.

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : DVB-C J.83 A/C, Cable Modulator J.83 B and DVB-T/H - contact us at info_cores@mvd-fpga.com
Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.

