



**Features**

Transmit side Udp / Ip / Mac stack, a real time UDP offload engine

- Drop-in module for Virtex-5™, Virtex-4™
- Programmable UDP source and destination ports
- Programmable IP source and destination addresses
- Programmable MAC destination address
- Configurable MAC source address
- Support JUMBO frame in option
- Clock up to 125 MHz for Virtex-4/5™
- Netlist version available for ISE 8.2 and later

**Description**

The MVD “UDP Transmit engine” core is a drop-in module that includes the following functions :

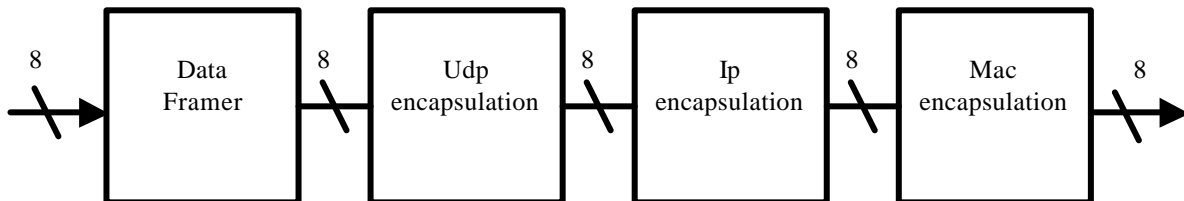
- Full hardware UDP encapsulation
  - Full hardware IP encapsulation
  - Auto-increment of the identification IP field
  - IP fragmentation not supported
  - Directly compatible with the XILINX TEMAC
  - Programmable with a Microblaze or a PPC405
- Up to 450 Mbits/sec

Design up to 125 MHz for Virtex-4/5™.

**Applications**

MVD Hw UDP stack may be used in applications related to Ethernet transmission, especially with XILINX FPGA technology

MVD can also provide additional remote or on-site support or cores for UDP Rx, ARP, ICMP, DHCP ...



**Resource Utilization**

	Slices	BRAMs	BUFG	Deliverables Netlist for core generation and simulation : ISE 8.2, 9.1, 9.2
Virtex 4	650	2	1	
Virtex 5	580	1	1	

**Ordering information and related cores**

Netlist version : MVD\_UDPTX\_NET\_8.2  
 Netlist version : MVD\_UDPTX\_NET\_9.1  
 Netlist version : MVD\_UDPTX\_NET\_9.2

Related cores : UDP Receive engine, ARP hardware module, MPEG-TS framer, ... (VHDL or netlist versions) contact us

