Implementing a Digital Video Broadcasting (DVB) or CMTS modulators with low cost FPGAs ? Let MVD do the job !

MVD remultiplexer and modulators solutions for DOCSIS, EURODOCSIS, DVB-C (J83A/C),Cable Modulator (J83B), DVB-S, DVB-T and DVB-H

1. Introduction

Digital Video Broadcasting and CMTS modulation involve many different processes and techniques, each of them having to comply with the respective standards. Those processes include frame processing and PCR [Program Clock Reference] restamping, channel coding (energy dispersal, Reed Solomon, interleaver, Forward Error Correction, Symbol Mapping and others) as well as Digital Signal Processing like filters, Inverse FFT, interpolation and Intermediate Frequency modulation.

When starting a modulator or transmodulator design, the following questions come up :

- If I buy a core for FPGAs, how long will it take to implement it successfully ?
- I'm not very familiar with FPGAs, and wouldn't like to spend too much time in finding the way to check the compliance of my modulator to the standards.

☞ **The ready-to-use MVD's modulators core family is the correct answer.**

Figure 1 shows a typical block diagram of a generic modulator

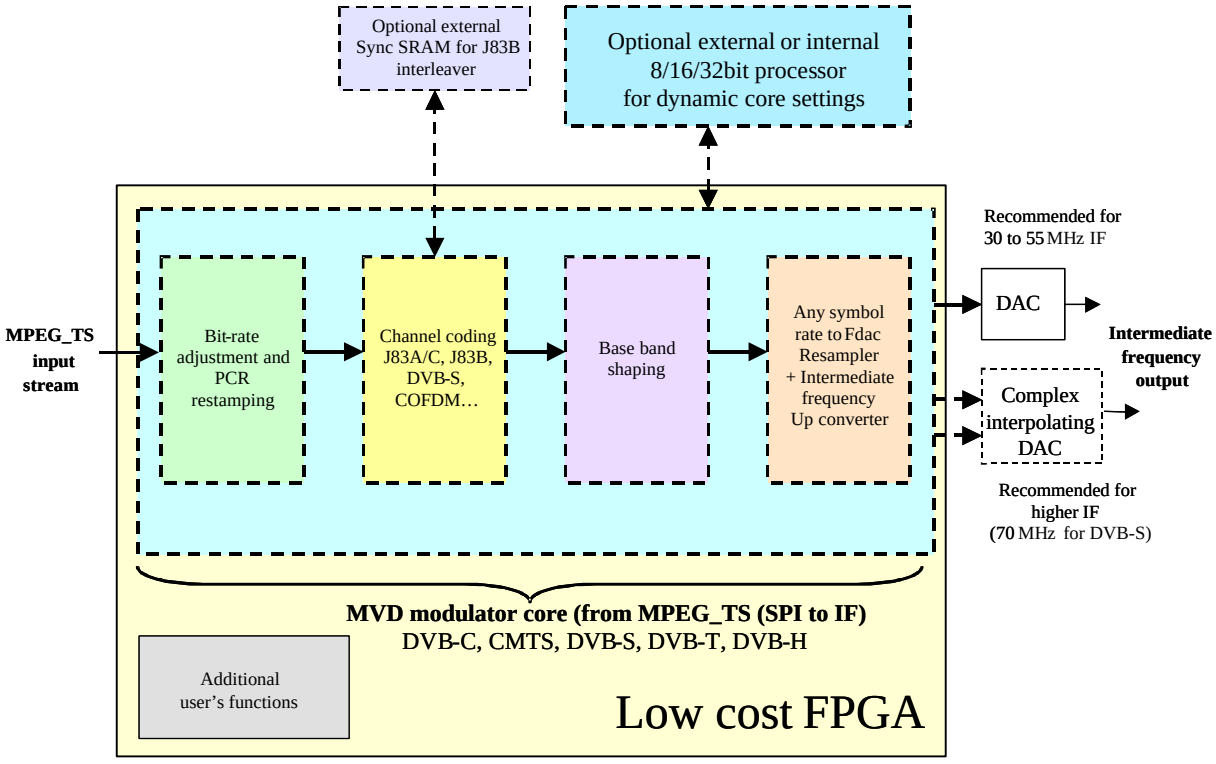


Figure 1 - block diagram of a typical modulator. It includes all digital processing functions from MPEG_TS (also called SPI) to Intermediate Frequency.

2. The modulator

The modulator itself contains various units.

2.1. The modulation process

A typical modulator includes the following steps sub-units:

- Bit rate adjustment and PCR correction :
  for determined modulator settings, the bit rate must be regulated to the exact value needed by the modulator. Null packets insertion (or sometimes removal), allows to maintain the right bit rate at the channel coding input. Of course, each time the original MPEG_TS stream is modified by inserting or removing null packets, PCRs fields must be corrected.

☞ **MVD modulators cores provide such bit rate adjustment with PCR correction, so the user doesn't have to worry about the understanding of how to implement this function.**

- Channel coding :
  Depending on the modulator type, many channel coding schemes are applied for compliance with he required standard. Some common standards are :
  - J83A/C used for cable modulators in Europe and ASIA
  - J83B use for cable modulators in USA
  - DVB-S
  - DVB-T
  - DVB-H

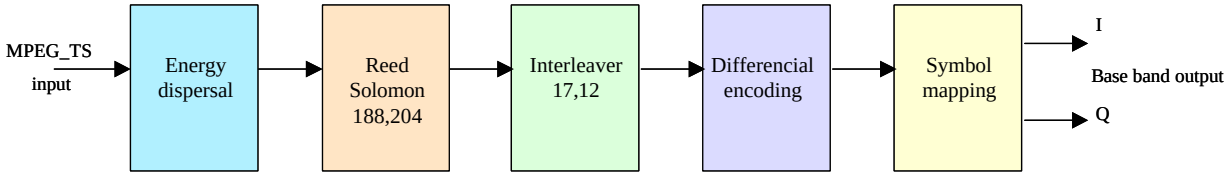


Figure 2 - Block diagram example of a J83A/C channel coding block

☞ **MVD cores offer full compliance with the J83A/C, J83B, DVB-S, DVB-T and DVB-H standards and their options.**

- Base band shaping :
  According to the type of modulator and corresponding standards, the base band I and Q signals coming from the channel coding module must be "shaped", so its spectrum complies with the required standard.
  Typically this is implemented by using FIR filters. The number of taps can vary between 100 and 200 taps, depending on the needed performance. In some cases, it's also important to provide various different shaping filters, for more flexibility.

☞ **Base band shaping is included in all MVD modulators cores. MVD uses optimization techniques to minimize the FPGA logic resources while providing the flexibility of changing the filter coefficients.**

- Any symbol rate to Fdac resampler/interpolator + Intermediate Frequency modulation:
  In most modulators, the symbol rate can have many different possible values. On the other hand, the simplest way to use the DAC for intermediate frequency consists in implementing a low skew oscillator at a frequency between 120 and 160 MHz. For highest frequencies, it's recommended to use an interpolating DAC to allow reasonable data rate between the FPGA and the DAC, while using higher DAC frequencies.
  In any case, an adaptive resampling of the I and Q signals at the selected symbol rate must be implemented to sample the correct values with the DAC clock.

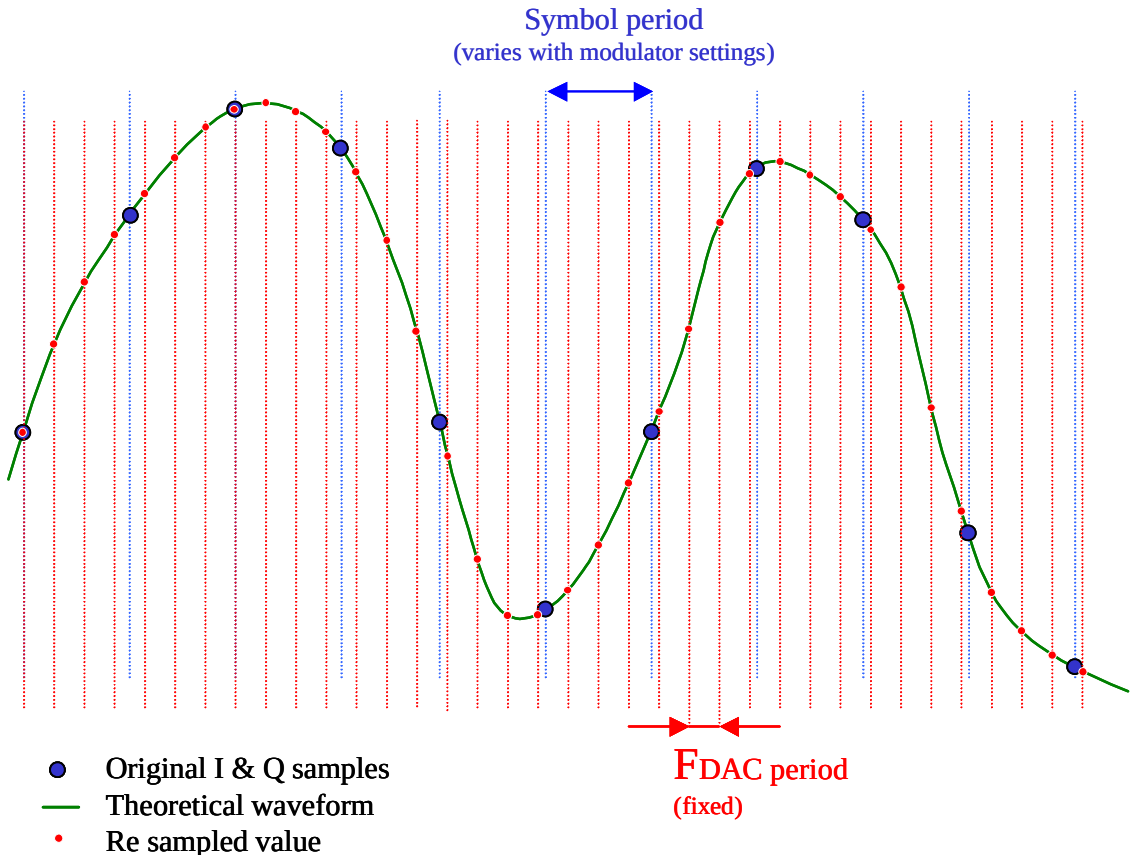


Figure 3 - Resampling base band I and Q signals to Fdac

If for example the symbol rate is 6.875 MHz and the DAC sample frequency 125 MHz, the needed interpolation factor is 18.181818 which is a non integer value This kind of programmable and non integer interpolation can't be implemented by using traditional techniques.
This is achieved by reconstructing the theoretical waveform with available I & Q samples, and then by resampling it at the Fdac sample frequency.
After being re-sampled, the new base band I and Q signals can be modulated to the Intermediate Frequency.

☞ **Just as bit rate adjustment and PCR restamping and base band shaping, the resampler and modulation functions are part of the MVD modulators cores.**
No need for the user to implement any other function for getting the complete modulator solution.

2.2. How to choose the right working frequency ?

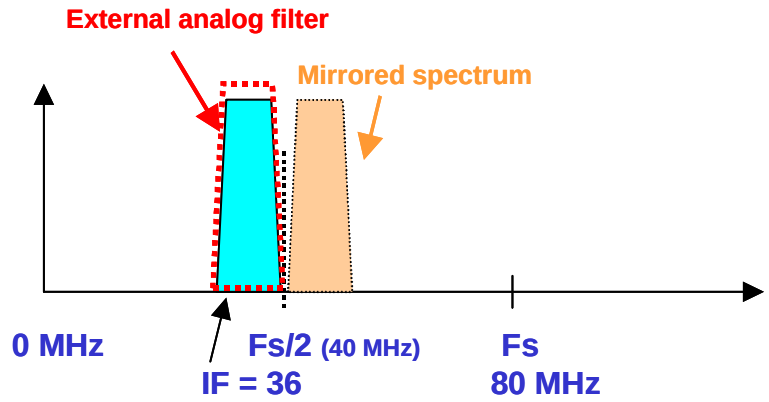
Only one clock is used in the MVD cores, in order to simplify the core implementation to its customers, with a 100% synchronous approach. By using this technique, only one clock tree and BUFG are needed for the complete core, and then there is no need of managing multi clock domain transfers.

In addition, MVD modulator cores have been optimised for using the minimum number of the FPGA logic resources, while reaching and overcoming the required performance. For example, base band processing is implemented by using time multiplexed resources in such a way that a 112-Tap filter (RRC) can be implemented by using only 4 DSP blocks working at Fsymbol x 14 (7MHz x 14 = 96 MHz). Note that coefficients symmetry is also taken in account.

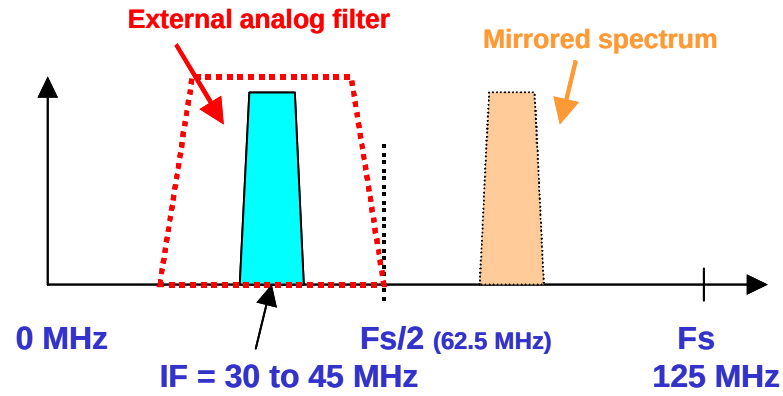
As low cost FPGA like Spartan3 families can internally work at 120 MHz to 140 MHz or more, using a reasonable high working frequency allows to reduce the FPGA size, and then helps to dramatically reduce the costs. By using such development techniques, a DVB-C (J83A/C) fits into a 3S400A or 3S500E !

Now, another consideration must also be considered : In most applications, the core must generate an Intermediate Frequency output. Usually, the IF frequency is around 30 to 45 MHz (most often 36 MHz), for a bandwidth of 6 to 8 MHz. This means that the useful spectrum can reach up to IF + BW/2 = 49 MHz for an intermediate frequency of 45 MHz and a bandwidth of 8 MHz. Theoretically a working frequency of 98 or 100 MHz would be sufficient to represent the wanted spectrum. However, this would require a very sharp and expensive analog filter to remove the image of the useful spectrum.

Taking in account the capabilities of the low cost Spartan-3 FPGAs, the resources optimisation techniques in order to reduce the overall costs, MVD Cores strongly recommend to use a working frequency in the range 120 to 140 MHz, typically 125 MHz. This allows for a very good optimisation of the resources used while easily meeting timing constraints and reducing the cost of the analog filter in charge of suppressing the mirrored spectrum.



Example 1 : Fs = 80 MHz. 36 MHz Intermediate Frequency is still possible, but very high performance is needed on the external filter. In addition, time sharing of the FPGA resources will be of poor effect due to the low working frequency used.



Example 2 : Fs = 125 MHz. 50+ MHz Intermediate Frequency is supported, even with using a low performance on the external analog filter. Time sharing of the FPGA resources is greatly improved due to the highest ratio between the Symbol Rate and the working frequency.

2.3. Configuring the modulator

MVD modulator cores can be configured by using a very simple 32-,16- or 8-bit microprocessor interface. The list of read/write registers is included in the cores datasheets.
MVD provides as an option RS232 and I2C interfaces, for customers that do not want to use the standard microprocessor interface.
If the RS232 interface is used, MVD provides a communication software that allows to configure the available options of each core.

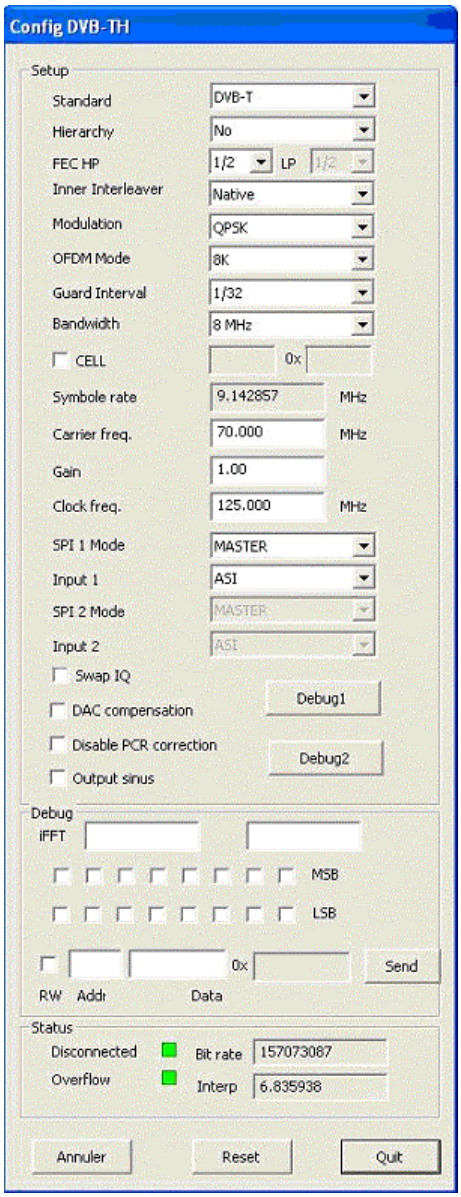


Figure 4 - MVD DVB core configuration software (Windows XP, Windows Vista)

2.4. What does the user have to do for implementing the complete modulator design ?

☞ **MVD modulator cores are ready to use solutions. No engineering is required from the user.**

The modulator cores can be delivered as netlist or simply as bitstream for the targeted FPGA, in order to use it just as a 100% functional dedicated integrated circuit.

☞ **MVD provides a free technical assistance to define the FPGA pinout for easy and efficient PCB routing.**

3. MPEG_TS frame processing (also called Remultiplexer)

In some applications – QPSK to COFDM transmodulation for example - the available MPEG_TS transport stream rate can be larger than authorized by the modulator. In such application, it is required to reduce the flow from 60 Mbits/sec to 30 Mbits/sec or less depending on the modulator settings.
This operation requires identifying all programs available in the input stream, in order to enable the installer to select the programs to be sent to the modulator, by taking into account the available bandwidth
Of course, after having selected the services to be transmitted, a new MPEG_TS stream must be reconstructed by reassigning valid PAT, SDT and as well as PCR fields. To comply to the new network distribution a new NIT (Network Information Table) is generated.
As the original MPEG_TS stream (coming from a QPSK demodulator for example) doesn't guarantees a smooth stream for any service, it's important to implement a "smoothing FIFO" thus allowing to regenerate a valid stream to transmit the selected programs, independently of their distribution and variations in the original stream. An external synchronous SRAM can be used for greater FIFO depth.

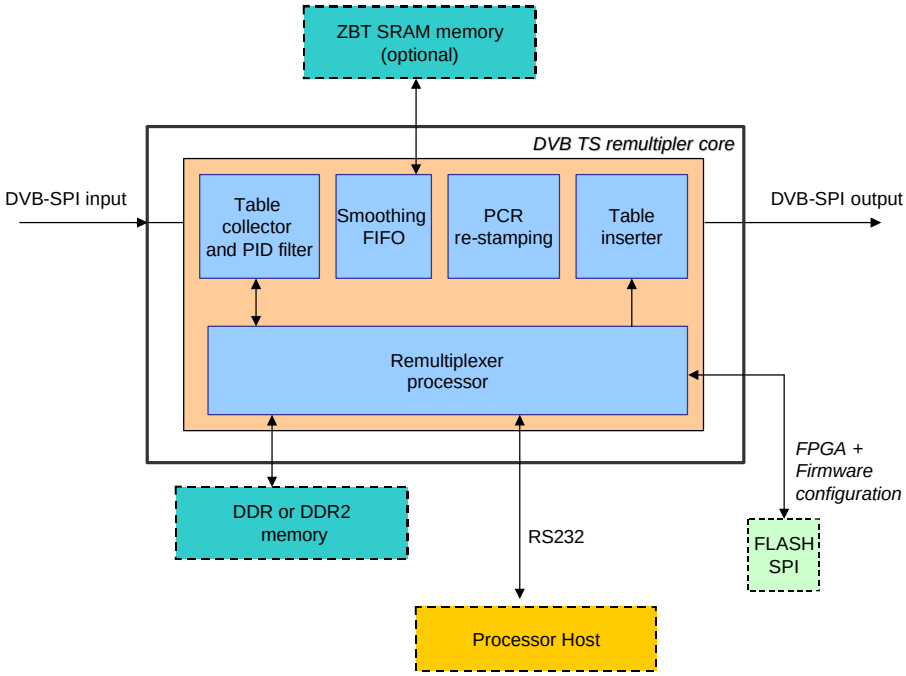


Figure 5 - Remultiplexer block diagram of a typical modulator.

☞ **The MVD remultiplexer core implements all those tasks. A dedicated microprocessor is used for packet fields management and user/installer interface. The installer can select the programs to be transmitted by using a computer with RS232 interface. MVD provides the application software at no extra cost. It runs on Windows XP and Windows Vista.**

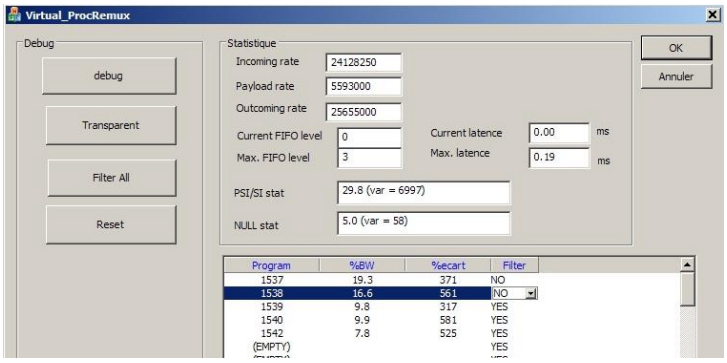


Figure 6 - Control window of the Remultiplexer

☞ **The MVD Remultiplexer core for FPGAs can be used as just a specific integrated circuit. No glue logic or engineering resources are needed.**

Just like for the modulator cores, the Remultiplexer core can be delivered as a bitstream for the targetted FPGA, ready to use on its PCB.

4. Transmodulation

A typical transmodulator (ex: QPSK to COFDM) includes both the Remultiplexer and the COFDM (DVB-T/H) core.

☞ **The MVD cores have been designed so that they can be directly interconnected freeing the user from the design of a complex interface.**

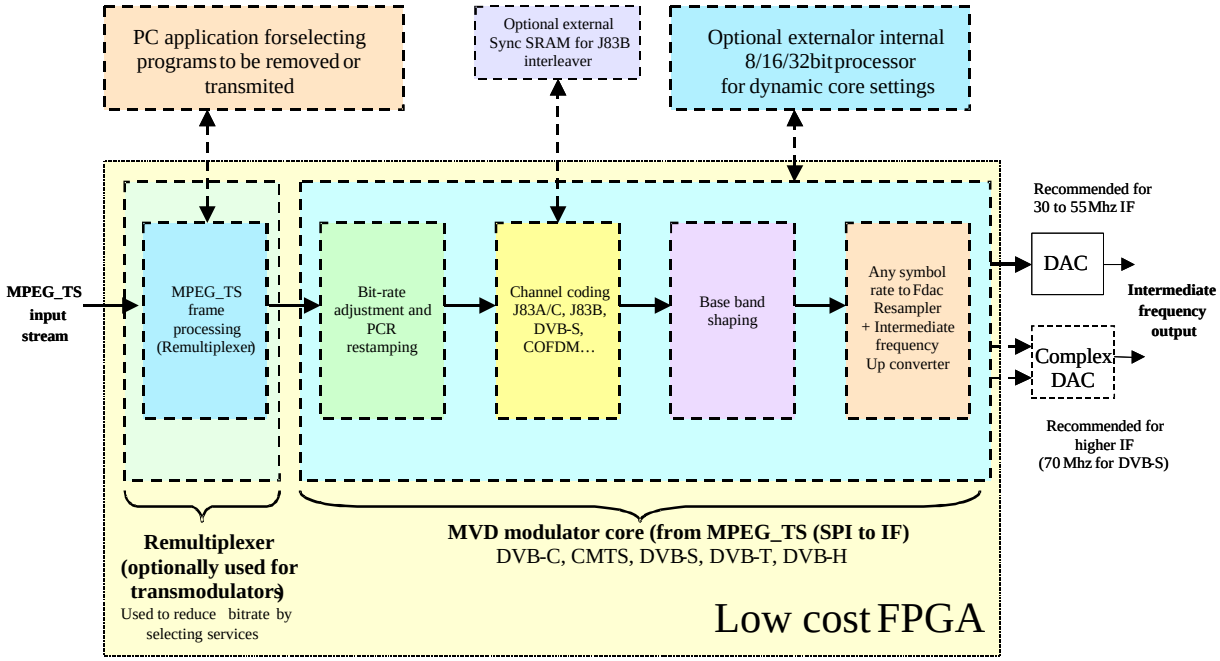


Figure 7 - block diagram of a typical transmodulator. It includes both Remultiplexer and Modulator cores.

MVD transmodulation solutions include the Remultiplexer core as well as the selected Modulator core. It can be delivered as a netlist, or as a bitstream.

☞ **For customers that choose the bitstream version of the cores, MVD provides pinout suggestions and technical assistance to take advantage of the FPGA flexibility in order to simplify the PCB design.**

5. Conclusion

MVD offers DVB-C, CMTS, DVB-S, DVB-T, DVB-H ready to use solutions for modulators and transmodulators, compliant to DOCSIS and EURODOCSIS .

☞ **Using MVD cores guarantees 100% successful designs without needing the knowledge of FPGA or modulator. For a smooth implementation, two days of remote technical support (email/phone) are included in the cores prices.**

For particular projects or conditions, customers may need some additional technical support for the cores implementation. MVD can propose this additional technical support remote or on site.

For any additional information, please have a look on our web site : **www.mvd-fpga.com**,
send us an e-mail at **info_cores@mvd-fpga.com**, or simply call us at the following number : **+33 5 62 13 52 32**