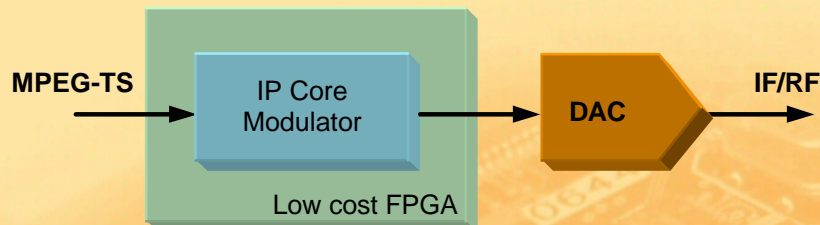


Digital Video Broadcast modulators

Modulator	Standard	Applications
DVB-T	ETSI EN 300 744 V1.5.1	<ul style="list-style-type: none"> - Digital terrestrial TV transmitter (MFN, SFN) - TV distribution system for hotels, resorts, apartments, hospitals, ... - Test equipment
ATSC	ATSC A/53 Part 2	<ul style="list-style-type: none"> - Digital terrestrial TV transmitter - TV distribution system for hotels, resorts, apartments, hospitals, ... - Test equipment
DVB-C	ETS 300 429 , ITU-T J.83 Annex A/C	<ul style="list-style-type: none"> - TV distribution system for hotels, resorts, apartments, hospitals, ... - Test equipment
J.83B	ITU-T J.83 Annex B	<ul style="list-style-type: none"> - TV distribution system for hotels, resorts, apartments, hospitals, ... - Test equipment
DVB-S	ETS 300 421	<ul style="list-style-type: none"> - Satellite TV base station - Test equipment



Main features	Supported Xilinx FPGAs	Supported DACs
<ul style="list-style-type: none"> - PCR re-stamping - IF or direct RF output (50MHz to 2GHz) - Single clock - Robust DVB-SPI input - Single or Multi-channel - MER > 40 to 43 dB 	<ul style="list-style-type: none"> - Spartan-3, Spartan-6 - Virtex-5, Virtex-6, Virtex-7 - Kintex-7 - Artix-7 	<ul style="list-style-type: none"> - AD9789 (Analog Devices) - AD9739 (Analog Devices) - AD9744 (Analog Devices) - MAX5881 (Maxim) - MAX5882 (Maxim) - MAX5879 (Maxim) - DAC5670 (TI) <p>Other DACs on demand</p>

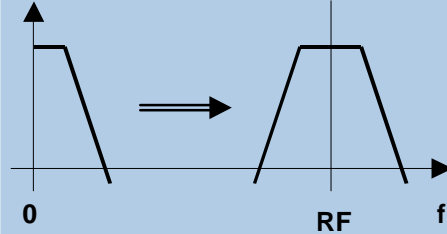
Benefits

- Complete modulator solutions (include PCR restamping, base band shaping, resampling)
- With our direct RF synthesis solutions, no need of an external analog Up Converter
- Minimized FPGA logic resources
- No engineering required from the user
- For a smooth implementation, two days (16 hours) of remote technical support (email/phone) are included in the cores prices.

Multi-channel Digital Up Converter for Direct RF Synthesis

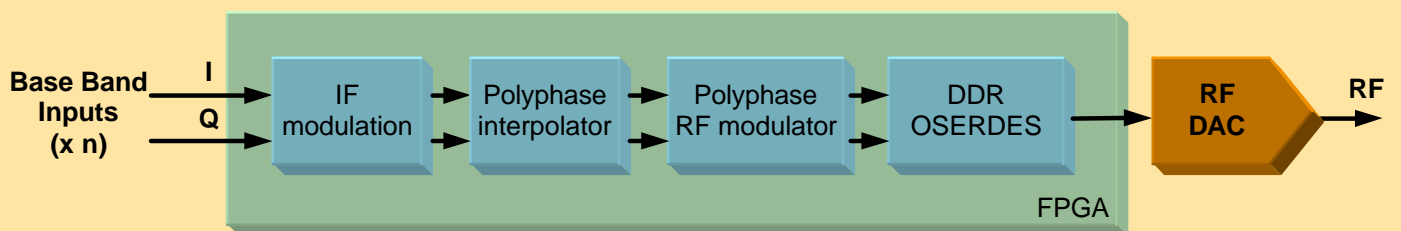
Function

Translation of a group of wide or narrow band channel into a wideband RF channel



Applications

- Broadband Communication Systems
- Cellular infrastructure
- Edge QAM devices
- Cable Modem Termination Systems (CMTS)
- Video-On-Demand (VOD)



Main features

- Totally scalable and adapted to customer's needs
- Single or Multi-channel
- RF output (50MHz to 2GHz)

Supported Xilinx FPGAs

- Spartan-6
- Virtex-5, Virtex-6, Virtex-7
- Kintex-7
- Artix-7

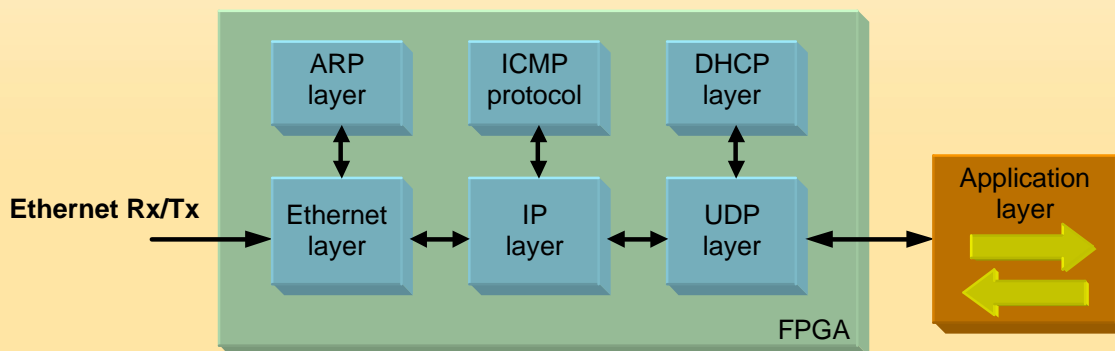
Supported DACs

- AD9739 (Analog Devices)
- MAX5881 (Maxim)
- MAX5882 (Maxim)
- MAX5879 (Maxim)
- DAC5670 (Texas Instruments)

Other DACs on demand

Full hardware UDP/IP Stack

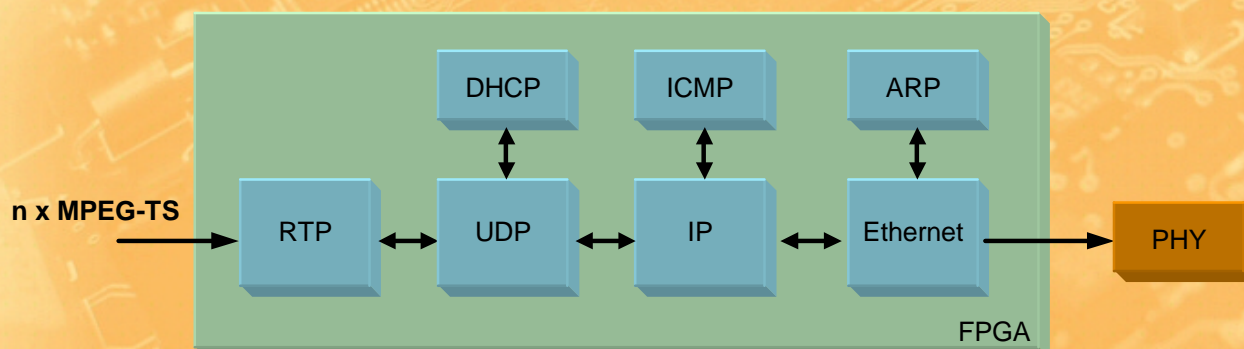
Supported protocols	Applications
<ul style="list-style-type: none"> - IPv4 - UDP - ARP - ICMP (Ping reply / Trace route) - IGMPv2 (option) - DHCP client (option) 	<ul style="list-style-type: none"> - High speed transfer between an FPGA and an Ethernet equipment



Main features	Supported Xilinx FPGAs
<ul style="list-style-type: none"> - Ethernet 100/1000 - UDP port filtering - CRC32 Ethernet validations - UDP/IP checksums validation 	<ul style="list-style-type: none"> - Spartan-6 - Virtex-5, Virtex-6, Virtex-7 - Kintex-7 - Artix-7

UDP/RTP Transmitter for IPTV

Supported protocols	Applications
<ul style="list-style-type: none"> - ARP - IPv4 - ICMP (Ping reply / Trace route) - UDP - MPEG2-TS UDP/RTP Transmission - Multicast Transmission - DHCP client (option) - FEC Protection (RTP Transmission only) (option) 	<ul style="list-style-type: none"> - TV distribution system on Ethernet network for hotels, resorts, apartments, hospitals, ...



Main features	Supported Xilinx FPGAs
<ul style="list-style-type: none"> - Ethernet 100/1000 - UDP port filtering - CRC32 Ethernet validations - UDP/IP checksums validation 	<ul style="list-style-type: none"> - Spartan-6 - Virtex-5, Virtex-6, Virtex-7 - Kintex-7 - Artix-7

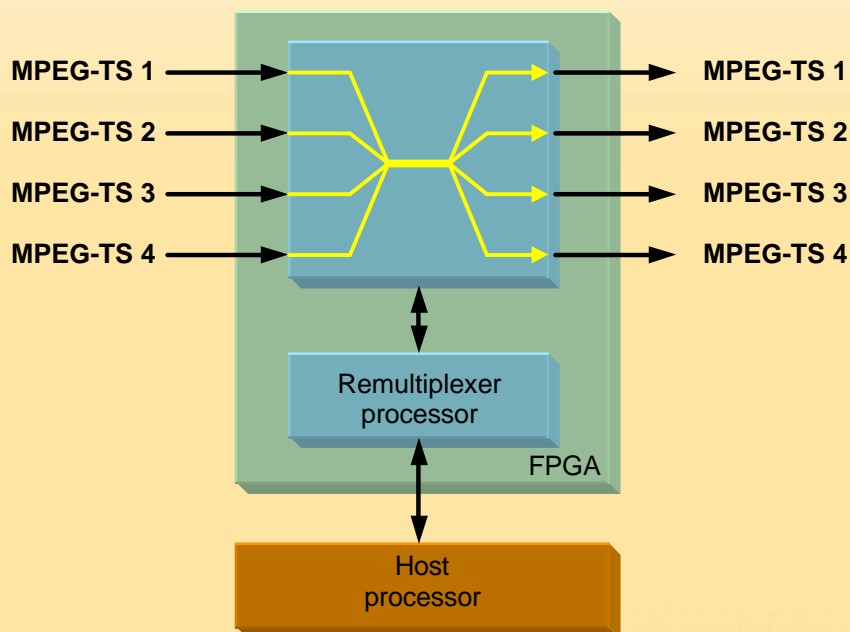
DVB Remultiplexer N-input to M-output

Function

Adapt one or several MPTS/SPTS stream into one or several MPTS by filtering and multiplexing complete services

Applications

- MPEG TS rate decrease by filtering services.
- Mixing satellite, terrestrial and local TV channels for hotels, resorts, apartments, hospitals TV distribution



Main features

- Up to 4 inputs, up to 4 outputs
- MPEG TS stream inputs analysis
- TS Stream information extraction
- User selected programs filtering
- Table regeneration
- SFN MIP table insertion independent for each output (for DVB-T core control)
- Configurable via an RS232 link or I²C link
- Full PCR re-stamping
- Statistical service bandwidth estimation per input
- CPU Interface to control MVD Modulator Core

Supported Xilinx FPGAs

- Spartan-3, Spartan-6
- Virtex-5, Virtex-6, Virtex-7
- Kintex-7
- Artix-7

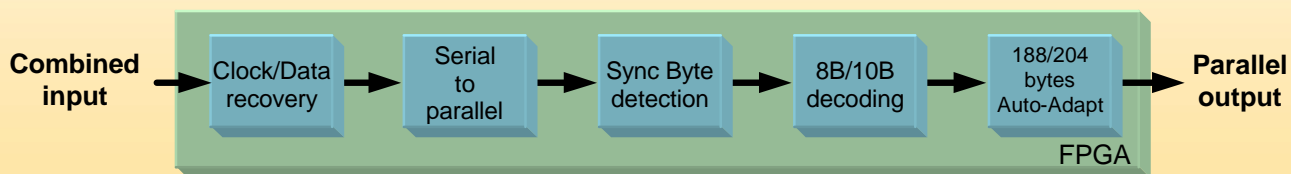
Supported standards

- UIT-T H222 (02/00) / ISO13818-1
- ETSI EN 300 468 v1.8.1 (2008-7)

Companion cores

ASI Receiver

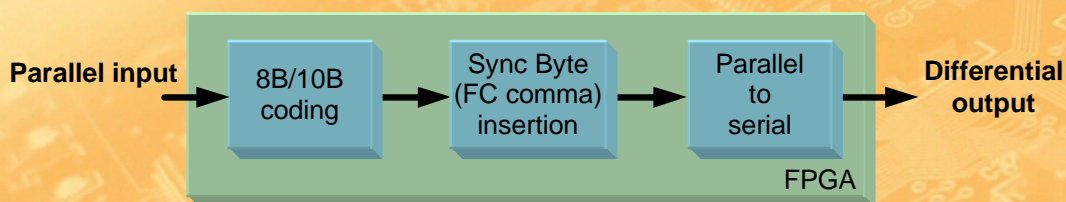
Function	Applications
Converts a DVB-ASI flow into a DVB-SPI flow	DVB/MPEG-2 TS Serial / Parallel Conversion



Main features	Supported Xilinx FPGAs
<ul style="list-style-type: none"> - 27MHz Single Clock - 188 or 204 bytes packet input - Direct ASI interface (clock recovery from Data) - Data Packet or Data Burst format 	<ul style="list-style-type: none"> - Spartan-6 - Virtex-5, Virtex-6, Virtex-7 - Kintex-7 - Artix-7
	Supported standards
	<ul style="list-style-type: none"> - EN50083-9 Annex B

ASI Transmitter

Function	Applications
Converts a DVB-SPI flow into a DVB-ASI flow	DVB/MPEG-2 TS Parallel / Serial Conversion



Main features	Supported Xilinx FPGAs
<ul style="list-style-type: none"> - 135 MHz Single Clock - 188 or 204 bytes packet input - Data Packet or Data Burst format - Choice of the output signal polarity 	<ul style="list-style-type: none"> - Spartan-3, Spartan-6 - Virtex-5, Virtex-6, Virtex-7 - Kintex-7 - Artix-7
	Supported standards
	<ul style="list-style-type: none"> - EN50083-9 Annex B

Companion cores (continued)

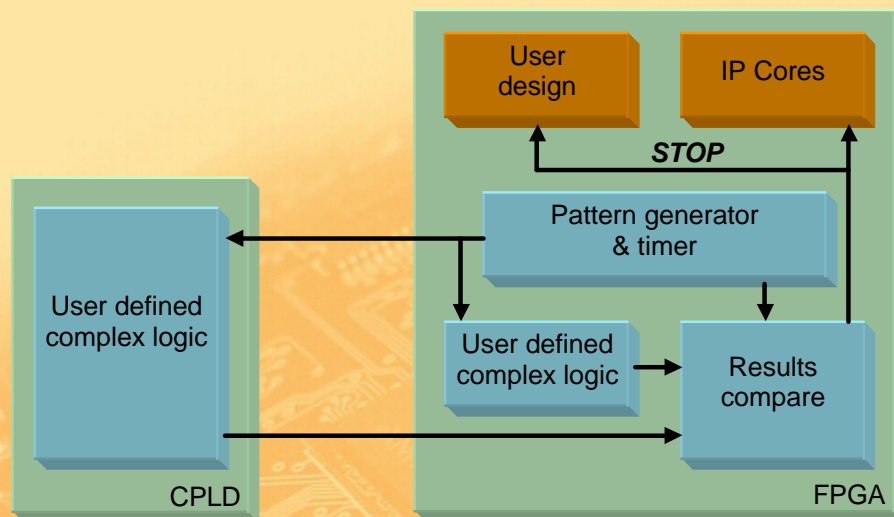
Serial Interface

Function	Applications
Parameters setting and status reading of MVD Cores modulators.	When local CPU is not available

Main features	Supported Xilinx FPGAs
<ul style="list-style-type: none"> - Input: Slave 400 KHz I2C interface for an 9-bit register or - Input: 9 600 or 115 200 Bauds UART interface, 8 bits, no parity, 1 STOP bit 	<ul style="list-style-type: none"> - Spartan-3, Spartan-6 - Virtex-5, Virtex-6, Virtex-7 - Kintex-7 - Artix-7

CPLD protection

Function	Applications
Protection against FPGA bitstream copy.	Counterfeiting prevention



Main features	Supported Xilinx CPLDs
<ul style="list-style-type: none"> - External encrypted CPLD - Source code of protection mechanism delivered - Customer chooses its own codes for the protection 	<ul style="list-style-type: none"> - CoolRunner-2

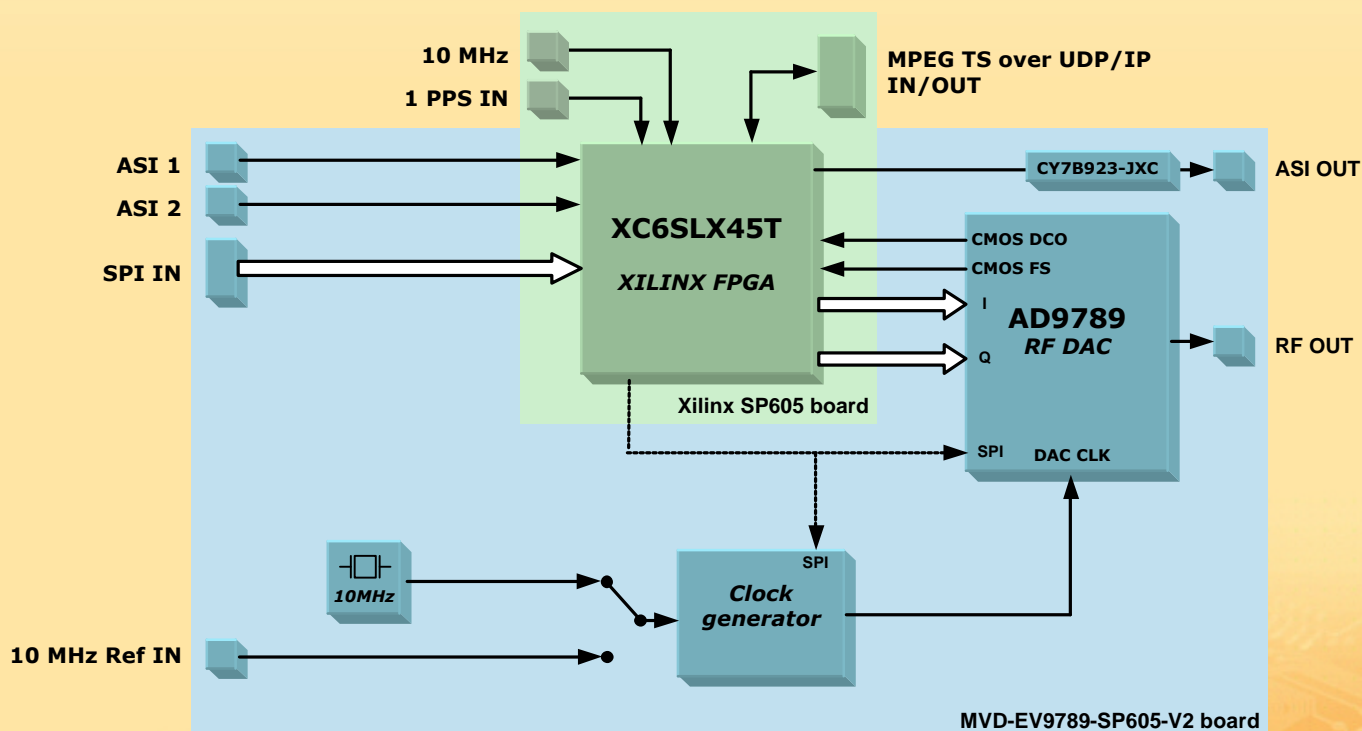
MVD-EV9789-SP605-V2 evaluation board

Function

The MVD-EV9789-SP605-V2 board converts an MPEG TS stream into an RF signal and supports most of the digital TV standards (DVB-C, J.83B, DVB-T, ATSC, DVB-S, ...).

Applications

The MVD-EV9789-SP605-V2 board is a daughter board for the SP605 Xilinx evaluation board. This pair of boards may be used for evaluation of MVD Cores' modulators/TS processing IP cores or as a test equipment for demodulation devices.



Main features

- FMC connector to connect to Xilinx SP605 evaluation board
- 1 x USB input for cores configuration
- 1 x 10 MHz Clock Ref input
- 1 x 1PPS input
- 1 x SPI (Synchronous Parallel Interface) TS input
- 2 x ASI (Asynchronous Serial Interface) TS inputs
- 1 x ASI (Asynchronous Serial Interface) TS
- 1 x MPEG TS over UDP/IP input/output
- 1 x IF/RF output (36 MHz to 1 GHz)
- "SFN Ready" for optional Single Frequency Networks

Supported Xilinx CPLDs

- MVD-EV9789-SP605-V2 board
- Documentation
 - o Hardware setup guide
 - o Schematics and PCB files
 Information you need to accelerate layout and development of your own board.

Xilinx SP605 board is not included. (available at www.xilinx.com)

Multi-Gigabit Serial I/O developments

Description

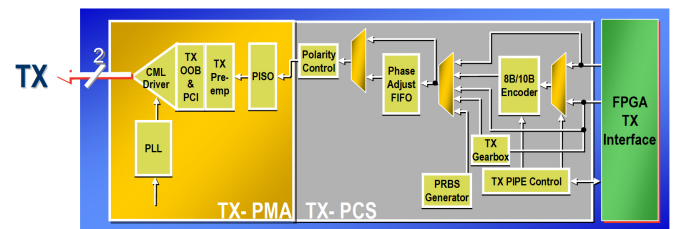
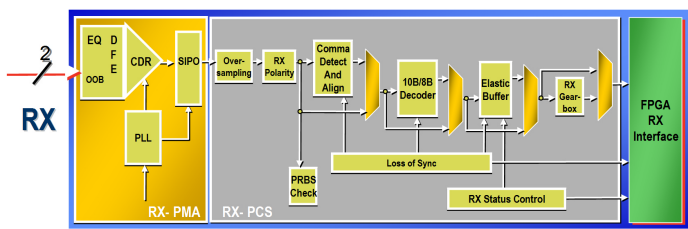
MVD Cores develops communication protocols for any proprietary high speed link including:

- Clock Configuration
- Clock/Data recovery
- Parallel/Serial, Serial/Parallel conversion
- Byte/Word alignment
- Channel Bonding
- Clock Correction
- Encoder/Decoder
- PRBS generator/checker
- Termination, Equalizer and Polarity Control

High speed serial applications

- Chip-to-chip
- Computing
- Datacom
- Storage
- Telecom
- Video

These developments can be based on high speed protocols such as **PCIExpress, Aurora, Gigabit Ethernet**, etc.



Main features

From 3.125 Gb/s with Spartan-6 LXT with GTP transceiver up to 28.5 Gb/s with Virtex-7 VH with GTZ transceiver

Supported Xilinx FPGAs

- Spartan-6
- Virtex-6
- Virtex-7
- Kintex-7
- Artix-7

Licensing

Our cores are sold at a fixed charge, royalty-free, independent of the production you can have. There are two possible licenses: **Project License** or **Site License**.

With the **Project license** you can use our core for one specific project (generally a project is defined by a model of printed circuit board). For this given project, you can implement several instances of the same core.

With the **Site license**, you can use our core for all the projects developed at your "site". Your "site" means a geographic location in which you conduct business, with a radius of no more than 5 miles.

Project license & Site license agreement templates are available on request.

Support

Several hours of remote technical support (email/phone) are included in the prices of our IP cores.

If needed, we can provide additional technical support (remote or on site). Support can include FPGA pinout, assistance for your board schematics, DAC configuration, ...

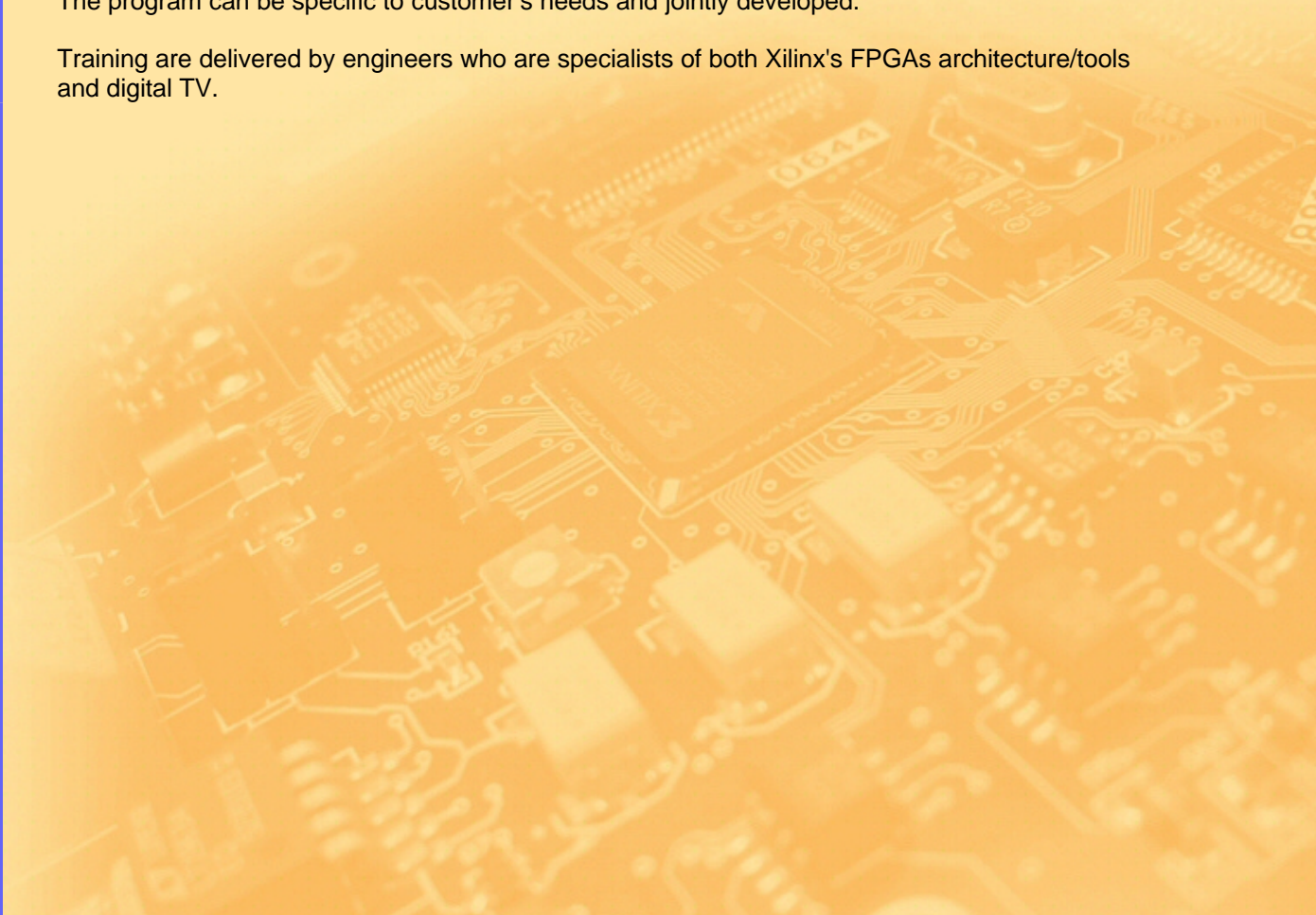
If your company doesn't want to spend engineering resources regarding the FPGA implementation, we can also deliver the entire FPGA project and bitstream.

Training

As an official partner of Xilinx, we can deliver on-site training at customer premises on Xilinx's FPGAs architecture and on Xilinx's implementation tools.

The program can be specific to customer's needs and jointly developed.

Training are delivered by engineers who are specialists of both Xilinx's FPGAs architecture/tools and digital TV.



About MVD Cores

Company profile

MVD Cores is an engineering team highly specialized in Digital Video Broadcasting (DVB) and FPGA technologies.

We provide IP cores for Xilinx FPGAs dedicated to MPEG TS processing, transporting and modulation (DVB, J.83B, ATSC, IPTV standards).

The products and services catalog contains a wide range of on-the-shelf IPs to build solutions to carry MPEG-TS to RF.

Our IPs cover almost all worldwide standards of current technologies for broadcasting over Digital Terrestrial Television (DTT), Cable TV (CATV), Satellite and IPTV.

Our IPs are easy to implement and ready to use. MVD Cores can provide technical support during all the design phases and will help you to use all the benefits of the FPGA by carrying out modular solution and scalable architecture. The expertise field covers optimized DSP functions for modulation, SERDES, high speed functions implementation, TS processing and System-On-Chip into the FPGA.

Our cores have been tailored to meet the requirements of most applications while using the lowest cost components and the lower amount of resources. However they can be adapted to specific needs.

MVD's cores enable its customers to build their high-end products while speeding up development phases.

Partners



MVD Cores is a Certified Member of the **Xilinx Alliance Program** and has demonstrated qualified expertise on the latest Xilinx devices and implementation techniques on Xilinx programmable platforms. As a Certified Member, MVD Cores has gone through a stringent certification process to ensure that our products and services are optimized to streamline customer product development cycles while minimizing risk.

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