**Features**

- European standard EN50083-9 Annex B
- Drop-in module for Spartan™-6, Virtex™-6, 7 Series and Ultrascale™ (+) Xilinx® FPGAs
- 135MHz Single clock
- Supports two type of inputs (DVB-SPI or "native")
- Supports Data Packet or Data Burst format
- Choice of the output signal polarity
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist

**Applications**

ASI Transmitter may be used in applications related to DVB/MPEG-2 transport streams.

**Description**

The MVD ASI Transmitter core is a drop-in module that includes the following functions:

- 188 or 204 bytes MPEG-TS input in DVB-SPI mode
- Any others data in "native" input mode
- 8B/10B Coding
- Sync Byte (FC Comma) Insertion
- Parallel/Serial Conversion
- Output signal polarity: normal or inverted

**Resource Utilization**

The core configuration may be set by conditional synthesis.

<table>
<thead>
<tr>
<th>Slices</th>
<th>Deliverables</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan-6</td>
<td>35</td>
</tr>
<tr>
<td>Virtex6, 7 Series</td>
<td>30</td>
</tr>
<tr>
<td>Ultrascale(+)</td>
<td>30</td>
</tr>
</tbody>
</table>

**Ordering information and related cores**

**Designation**

MVD_ASI_TX_NET

**VHDL source code**

can be delivered as an option under NDA and other specific clauses

**Related cores**

Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at info_cores@mvd-fpga.com