



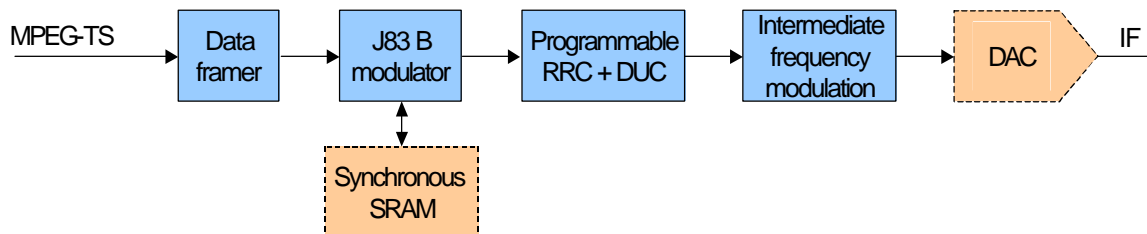
## Features

### ITU-T J.83 Annex B

Compliant baseband transmitter for Cable Modem Termination Systems (CMTS)

- Drop-in module for Virtex-5™, Virtex-4™ and Spartan™-3/E/A FPGAs
- Single clock (up to 140 MHz+ for Spartan-3™, 180 MHz+ for Virtex-4™ and Virtex-5™)
- Robust SPI input (discarding of incorrect input packets)
- PCR re-stamping
- Supports 5.056941 & 5.360537 symbol rates
- Programmable 64 and 256 QAM Symbol Mapping
- All interleaver modes supported thanks to external Synchronous SRAM
- Reduced interleaver modes can be implemented as internal memory
- Intermediate frequency output for single DAC (14 bits) or complex DAC (2 x 16 bits)
- Single channel – support for multi channel
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 43dB

Complete application fits into 3S500E and/or 3S400A depending on selected options



## Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU and external memory interface with all interleaver modes supported.

	Slices	BRAMs	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation
Spartan3/E/A	3 400	3	20	3	
Virtex 4	3 100	3	20	3	
Virtex 5	1 450	3	20	3	

*(values may vary depending on implementation options)*

Typical configuration with CPU interface and internal memory with 8K interleaver limitation.

	Slices	BRAMs	Mults/DSP48	BUFG
Spartan3/E/A	3 400	7	20	2
Virtex 4	3 100	7	20	2
Virtex 5	1 450	5	20	2

Typical configuration with CPU interface and internal memory with 32K interleaver limitation.

	Slices	BRAMs	Mults/DSP48	BUFG
Spartan3/E/A	3 400	17	20	2
Virtex 4	3 100	17	20	2
Virtex 5	1 450	10	20	2

Typical configuration with CPU interface and internal memory with all interleaver modes supported.

	Slices	BRAMs	Mults/DSP48	BUFG
Spartan3/E/A	3 400	31	20	2
Virtex 4	3 100	31	20	2
Virtex 5	1 450	17	20	2

### **Ordering information and related cores**

Parameters	Designation
Fixed	MVD_CMDLT_J83B_FIXED_NET
GPIO programmable	MVD_CMDLT_J83B_GPIO_NET
CPU programmable	MVD_CMDLT_J83B_CPU_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : J83B 4-Channel, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer and/or ASI Receiver cores  
contact us at [info\\_cores@mvd-fpga.com](mailto:info_cores@mvd-fpga.com)

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.