MVD Cores

IP core solutions for Digital Video Broadcasting

Digital Video Broadcast Modulators

Modulator	Standard	Applications	
DVB-T	ETSI EN 300 744 V1.5.1	Terrestrial TV transmitter (MFN, SFN)	DVB-T
DVB-T2	EN 302 755 V1.1.1	Terrestrial TV transmitter	DVB-T2
ATSC	ATSC A/53 Part 2	Terrestrial TV transmitter	
ISDB-T	ARIB STD-B31	Terrestrial TV transmitter	
DVB-C	ETS 300 429 , ITU-T J.83 Annex A/C	Cable TV transmitter	DVB-C
J.83B	ITU-T J.83 Annex B	Cable TV transmitter	
DVB-S	ETS 300 421	Satellite TV transmitter	DVB-S
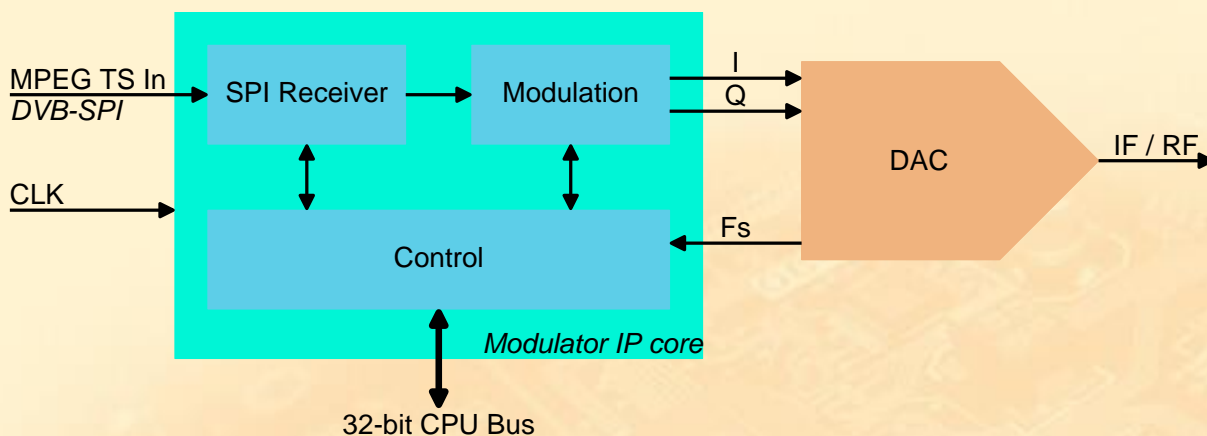
Main features

- PCR re-stamping
- IF or direct RF output (50MHz to 2GHz)
- Single clock
- Robust DVB-SPI input
- Single or Multi-channel
- MER > 40 to 43 dB

Supported Xilinx® FPGAs

- Spartan®-6, Virtex®-6
- Virtex®-7, Kintex®-7, Artix®-7
- Zynq®
- Ultrascale® / Ultrascale® +

Benefits

- Complete modulator solutions (include PCR restamping, base band shaping, resampling)
- With our direct RF synthesis solutions, no need of an external analog Up Converter
- Minimized FPGA logic resources
- No engineering required from the user
- For a smooth implementation, 3 months of remote technical support (email/phone) from delivery are included in the cores prices.
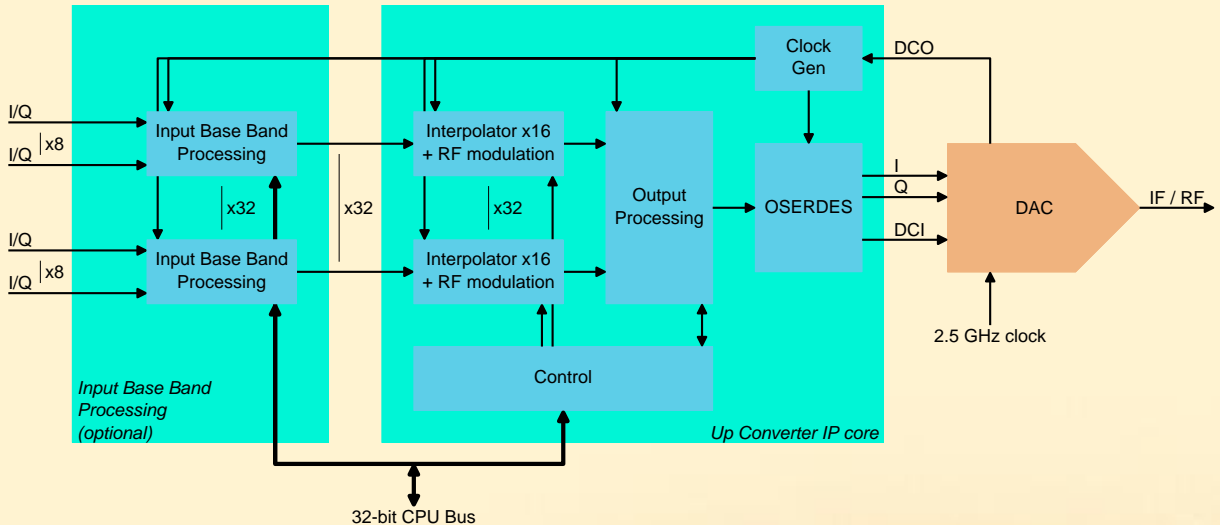
Signal processing

Multi-channel Digital Up Converter for Direct RF Synthesis

Function	Applications
Translation of a group of wide or narrow band channels into a wideband RF channel	- Broadband Communication Systems - Cellular infrastructure - Edge QAM devices - Cable Modem Termination Systems (CMTS) - Video-On-Demand (VOD)

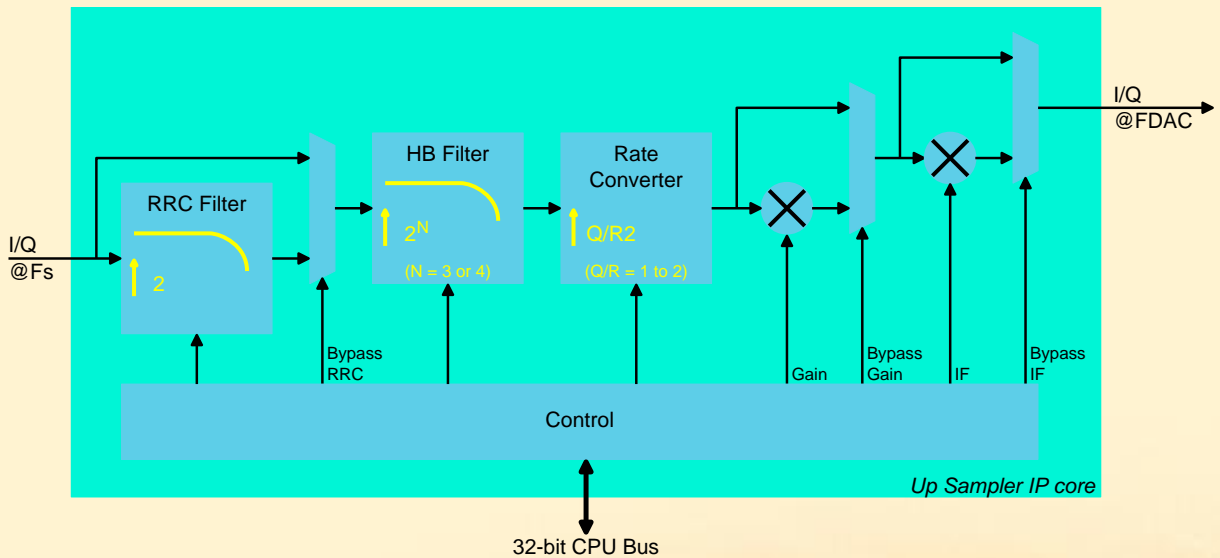| Main features	Supported Xilinx FPGAs
- Totally scalable and adapted to customer's needs - Single or Multi-channel - RF output (50MHz to 2GHz)	- Spartan-6, Virtex-6 - Virtex-7, Kintex-7, Artix-7 - Zynq - Ultrascale / Ultrascale +

Signal processing

Up Sampler

Function

Converts complex baseband I-Q signal @ Fsymbol rate to complex baseband or IF I-Q signal @ Fclock DAC

Applications

The UPSAMPLER is recommended for using DAC which has no up sampling stage. The application is for digital TV transmission system requiring low noise and filter adjustment stages.

RRC Filter
$\uparrow 2$

HB Filter
$\uparrow 2^N$
(N = 3 or 4)

Rate Converter
$\uparrow Q/R2$
(Q/R = 1 to 2)

I/Q @Fs

I/Q @FDAC

Bypass RRC

Gain

Bypass Gain

IF

Bypass IF

Control

Up Sampler IP core

32-bit CPU Bus

Main features

- Compliant with all our cable and terrestrial modulators
  (DVB-C J83A/C, J83B, ATSC, DVB-T/T2)
- Includes Symbol rate generator
- Programmable RRC filter for cable modulators
  (J83B : 0.12 or 0.18, DVB-C/J83A : 0.15, ISDBC/J83C : 0.13)
- Programmable symbol rates for cable modulators
  (from 5MSymb/s to 7MSymb/s)
- Programmable output bandwidth for DVB-T/T2 (5, 6, 7 or 8 MHz)
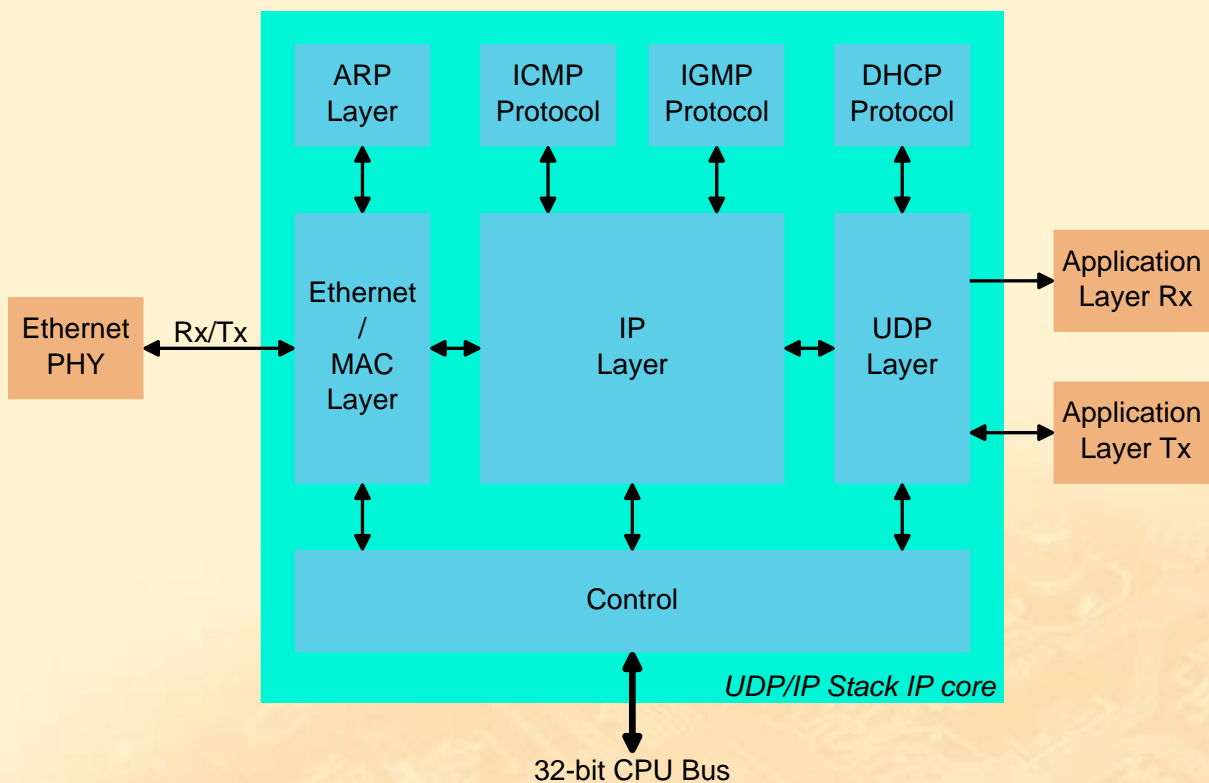- Complex baseband or IF outputs (2 x 16 bits) @ Fclock DAC

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

Ethernet

Full hardware UDP/IP Stack

Supported protocols

- IPv4
- UDP
- ARP
- ICMP (Ping reply / Trace route)
- IGMPv3
- DHCP client
- VLAN Rx / Tx (IEEE 802.1 Q Frame)

Applications

The UDP/IP core can be used in applications related to Ethernet transmission:
- voice over IP (VoIP)
- television over IP (IPTV)
- fast transmission of large amounts of data
  (medical imaging, etc)

UDP/IP Stack IP core

32-bit CPU Bus

Main features

- Ethernet 100/1000
- UDP port filtering
- CRC32 Ethernet validations
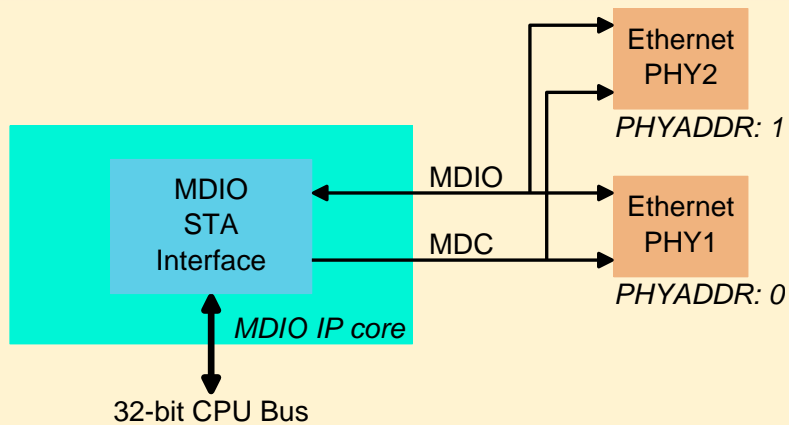- Support Multicast for both Reception and Transmission
- UDP/IP checksums validation

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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Ethernet

MDIO STA Management Interface

Function	Applications
Easy control of the Ethernet PHY	Control of external PHY Ethernet by writing and reading PHY's registers.

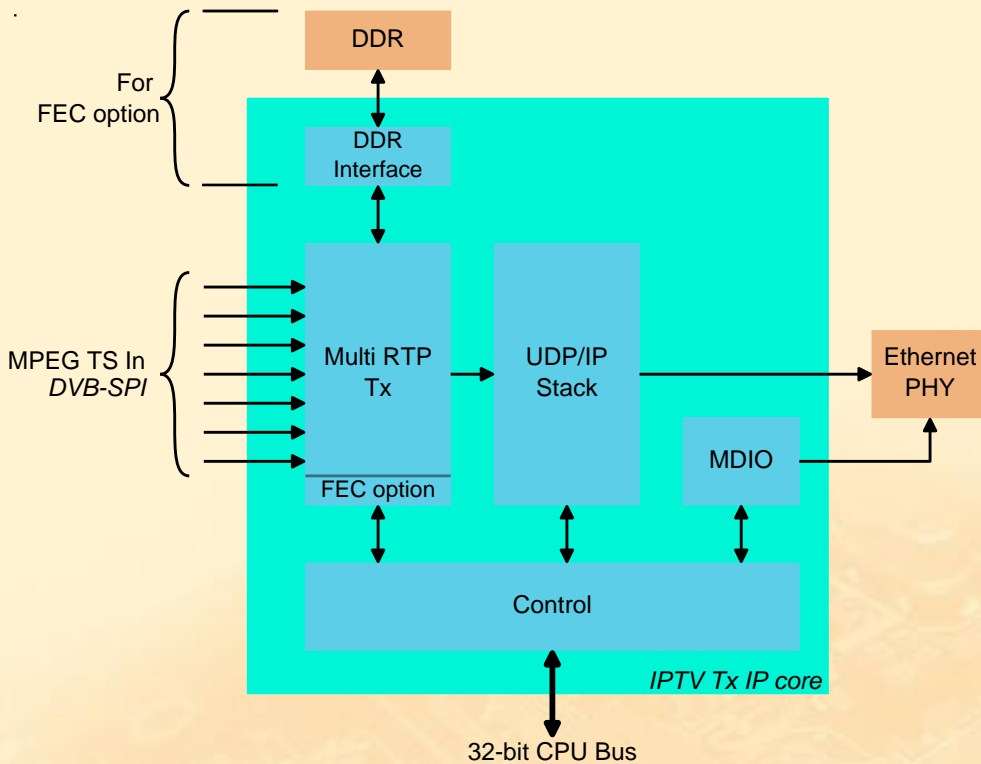| Main features	Supported Xilinx FPGAs
- Write / Read PHY Registers - MDIO Output Interface - MDC clock generation - Up to 32 components managed - IEEE 802.3 compliant	- Spartan-6, Virtex-6 - Virtex-7, Kintex-7, Artix-7 - Zynq - Ultrascale / Ultrascale +

IPTV Transmitter

Function

An **IPTV Transmitter** can be built from several MVD IP cores:
- **RTP Transmitter**
- **UDP/IP Stack**

The IPTV Transmitter gets one or several MPEG TS streams and sends them in UDP/RTP packets to an Ethernet link

Applications

TV distribution system on Ethernet network for hotels, resorts, apartments, hospitals, …

Main features

- For TS input only
- Sends IPTV packets UDP or RTP formatted
- FEC (Forward Error Correction) to prevent packets loss in a routed network (Compliant with the SMPTE 2022-1-2007)
- Seamless switching support SMPTE 2022-7

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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Ethernet

IPTV Receiver

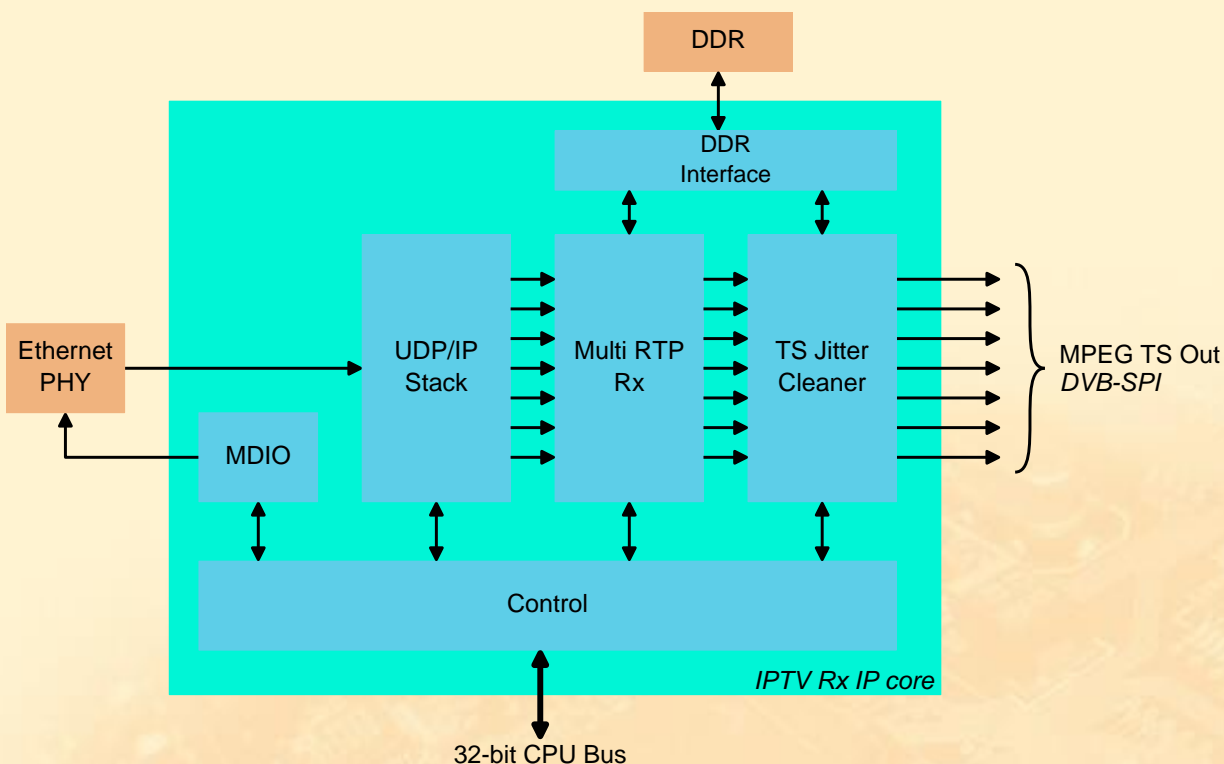| Function	Applications
An **IPTV Receiver** can be built from several MVD IP cores: - **UDP/IP Stack** - **RTP Receiver** - **TS Jitter Cleaner** (deburst/dejitter) The IPTV Receiver extract one or several MPEG TS streams (CBR) from UDP/RTP packets from an Ethernet link and sends them to DVB-SPI outputs	TV distribution system on Ethernet network for hotels, resorts, apartments, hospitals, …

Main features	Supported Xilinx FPGAs
- Can support up to 64 input streams - Automatic detection of input packet type (UDP or RTP) - Dejitter and deburst incoming CRB IPTV streams	- Spartan-6, Virtex-6 - Virtex-7, Kintex-7, Artix-7 - Zynq - Ultrascale / Ultrascale +

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Ethernet

SAP/SDP Inserter

Function

Allows to send SAP/SDP packets for multicast stream announcements.

Session Announcement Protocol (SAP) is a protocol to broadcast multicast session information. SAP was published by the IETF as RFC2974.

The core encapsulates Session Description protocol (SDP) as a description of streaming media information.
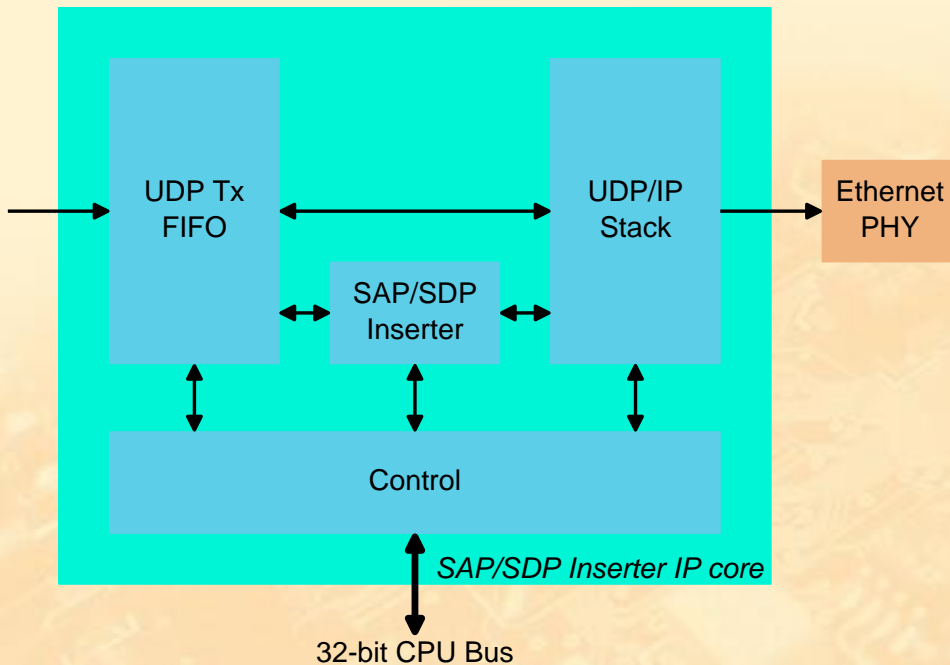SDP was published by the IETF as RFC4566.

SAP/SDP inserter sends periodically SAP/SDP announcements at Multicast address 239.255.255.255 and UDP port 9875.
These announcements allow the receivers which support SAP/SDP protocol to retrieve all the necessary information to connect to all streaming multicast media present.

Applications

Add-on module for the MVD UDP/IP Stack for multicast stream announcements on a local network.

```
           ┌─────────┐              ┌─────────┐     ┌──────────┐
     ──────▶│ UDP Tx  │◀───────────▶│ UDP/IP  │────▶│ Ethernet │
           │  FIFO   │              │  Stack  │     │   PHY    │
           └─────────┘              └─────────┘     └──────────┘
                │     ┌──────────┐        │
                │  ◀─▶│ SAP/SDP  │◀─▶     │
                │     │ Inserter │        │
                ▼     └────┬─────┘        ▼
           ┌──────────────┴───────────────────┐
           │            Control                │
           └───────────────────────────────────┘
                         SAP/SDP Inserter IP core
                          ↕
                    32-bit CPU Bus
```

Main features

- Generates SAP Header and encapsulates SDP data into SAP packets
- SDP description (ASCII) is sent through CPU interface
- Can support up to 128 SAP/SDP Channels
  (if more channels are required please contact MVD)

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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Ethernet

Unidirectional Lightweight Encapsulation (RFC4326) Encoder

Function

Insert IP packets into user MPEG-2 TS according to RFC4326 standard.

Applications

Tansportation of network layer packets over MPEG transport stream with low overhead.

IP Packets In
RAW

RFC4326
Encoder

MPEG-TS Out
DVB-SPI

*RFC4326 Encoder
IP core*

32-bit CPU Bus
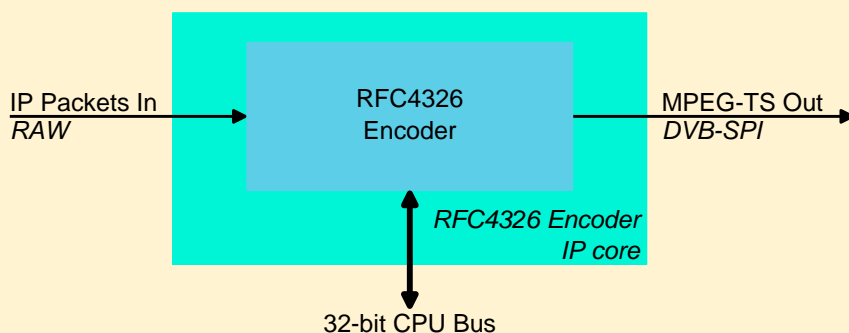
Main features

- IP Packets encapsulation in TS frame in completion or no completion mode
- Output in 188 or 204 byte CBR mode (with RS188/204 encoded byte)
- PAT/PMT generation
- Custom PID for PMT and PAYLOAD frames
- Custom PSI generation delay
- Configurable output rate

Supported Xilinx FPGAs

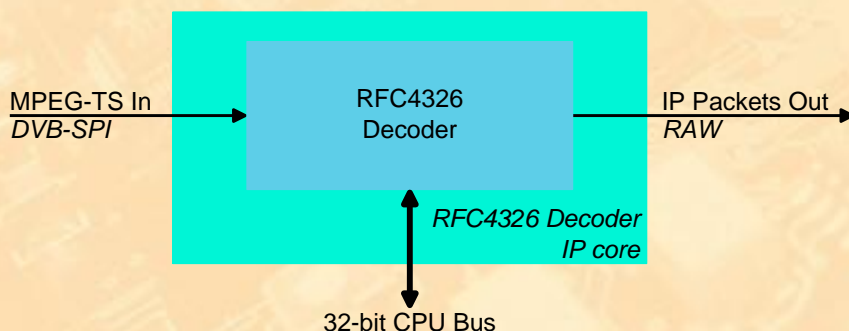- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq

Unidirectional Lightweight Encapsulation (RFC4326) Decoder

Function

Extracts IP packets from user MPEG-2 TS according to RFC4326 standard.

Applications

Tansportation of network layer packets over MPEG transport stream with low overhead.

MPEG-TS In
DVB-SPI

RFC4326
Decoder

IP Packets Out
RAW

*RFC4326 Decoder
IP core*

32-bit CPU Bus

Main features

- TS Frame de-encapsulation
- Automatic PAT/PMT analysis and PAYLOAD recovery
- ETR 101290 Alarms (continuity count error, locked length)

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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MPEG-TS Processing

DVB

DVB/ATSC Remultiplexer N-input to M-output

Function	**Applications**
Adapt one or several MPTS/SPTS stream into one or several MPTS by filtering and multiplexing complete services	- MPEG TS rate decrease by filtering services. - Mixing satellite, terrestrial and local TV channels for hotels, resorts, apartments, hospitals TV distribution
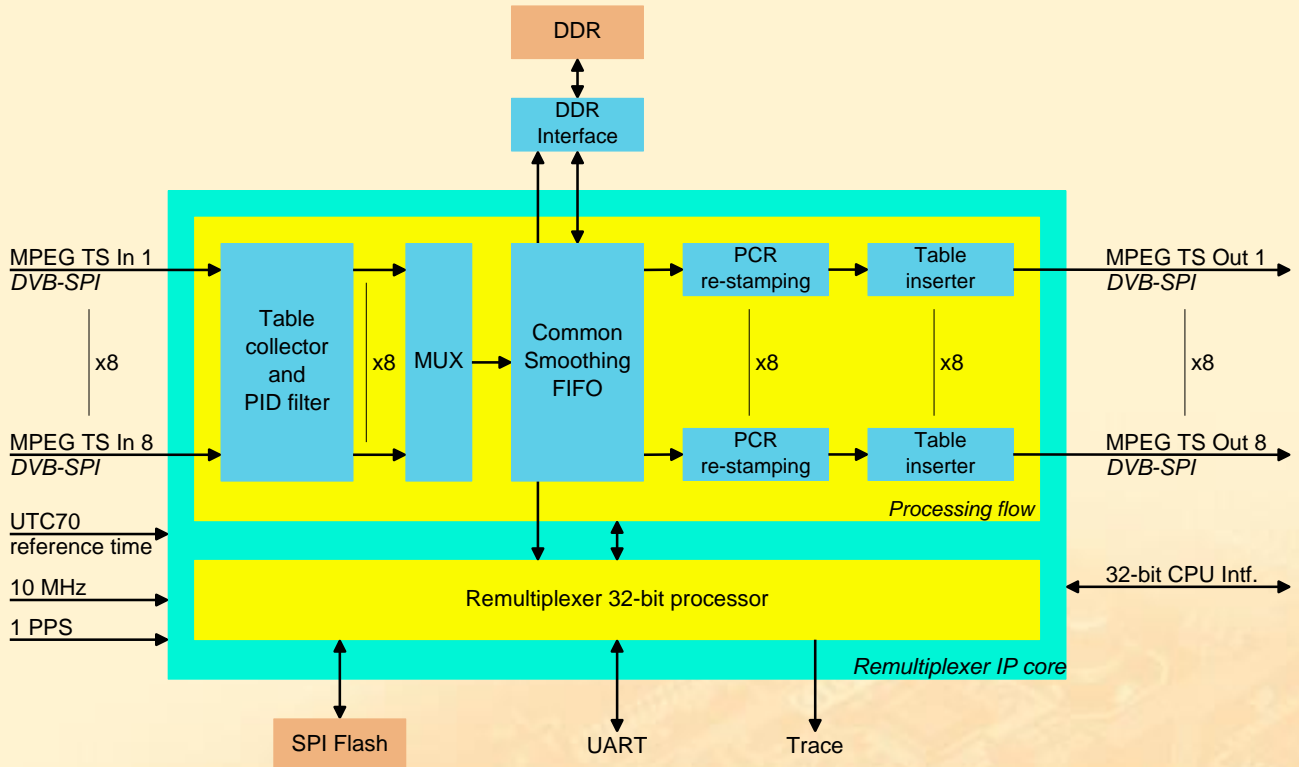
Main features

- Up to 8 inputs, up to 8 outputs
- MPEG TS stream inputs analysis
- TS Stream information extraction
- User selected programs filtering
- Tables regeneration
- EPG present/following and schedule
- SFN MIP table insertion independent for each output (for DVB-T core control)
- Configurable via an RS232 link or I²C link
- Full PCR re-stamping
- Statistical service bandwidth estimation per input
- CPU Interface to control MVD Modulator Core

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

Supported standards

- UIT-T H222 (02/00) / ISO13818-1
- ETSI EN 300 468 v1.8.1 (2008-7)
- ATSC A/65:2009
- A/53 part 3

MPEG-TS Processing

SPTS to MPTS Multiplexer

Function	*Applications*
ATSC or DVB standard mixing of up to 32 incoming SPTS stream	Applications related to transmodulation (from encoder to ATSC terrestrial channel or DVB-T terrestrial channel) or for video acquisition in case of completion of information.

SPTS to MPTS Multiplexer IP core

32-bit CPU bus

| *Main features*	*Supported Xilinx FPGAs*
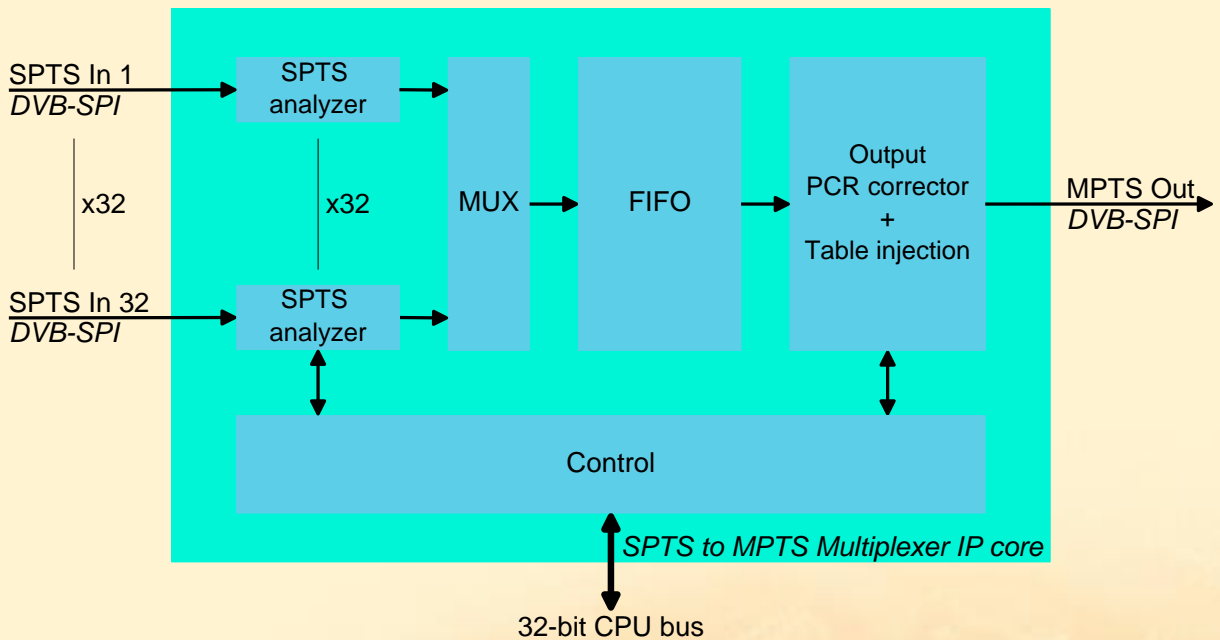
- Incoming stream analysis
- Capture of ATSC/PSIP or DVB/PSI/SI sections
- Capture of PMT sections
- Stream parameters extraction
- PSIP/PSI/PMT tables downloading
- Solving of serviceID and PID conflict between inputs
- Generation of output tables:
  • new PAT
  • VCT
  • SDT
  • Updated MGT and PMTs (when required)
  • PCR adaptation
	- Spartan-6, Virtex-6
	- Virtex-7, Kintex-7, Artix-7
	- Zynq
	- Ultrascale / Ultrascale +

MPEG-TS Processing

MPTS Demultiplexer

Function

Receives an MPTS input stream and de-multiplexes services according to the PID programming done.
Can de-multiplex up to 32 services with up to 32 PIDs per service.

Applications

Can be used in addition to the DVB/ATSC remultiplexer core and IP-TV transmitter for SPTS to IP application.

MPTS Demultiplexer IP core
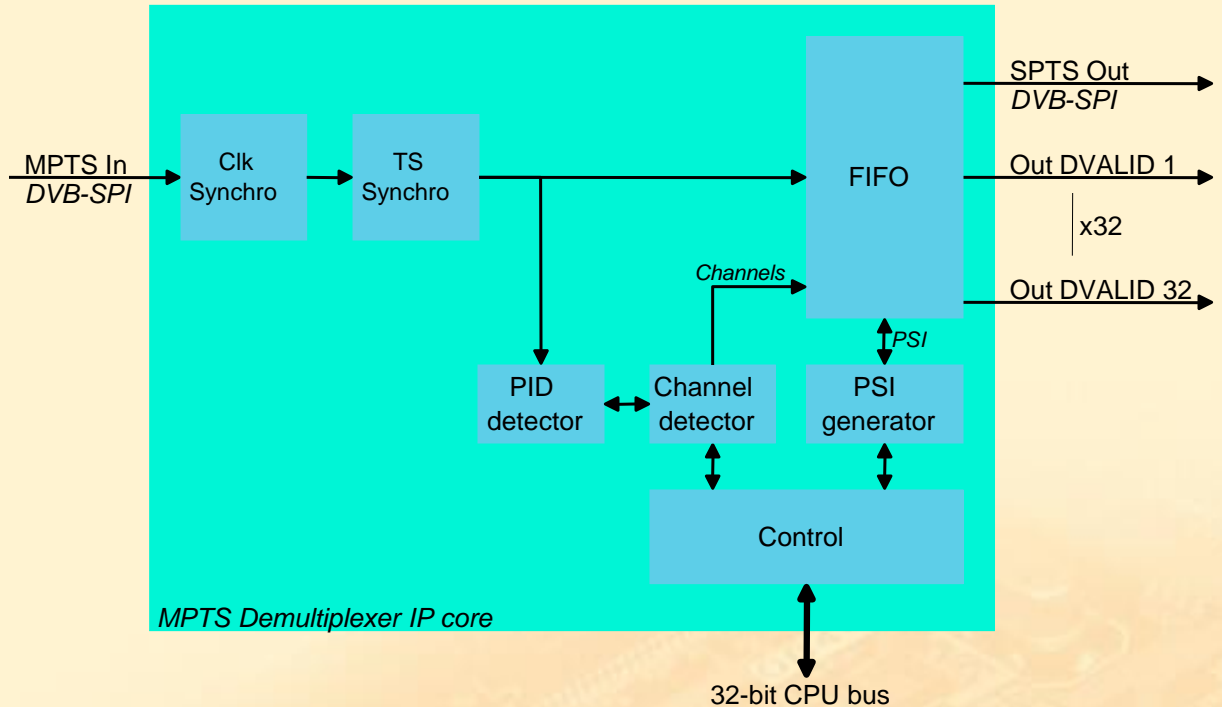
Main features

- De-multiplexes up to 32 services with up to 32 PIDs per service
- Automatic filtering of incoming tables (PAT, SDT, EIT , NIT)
- NULL packet deletion
- Passed through PMT without modification
- Regeneration of SDT and EIT for each services

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
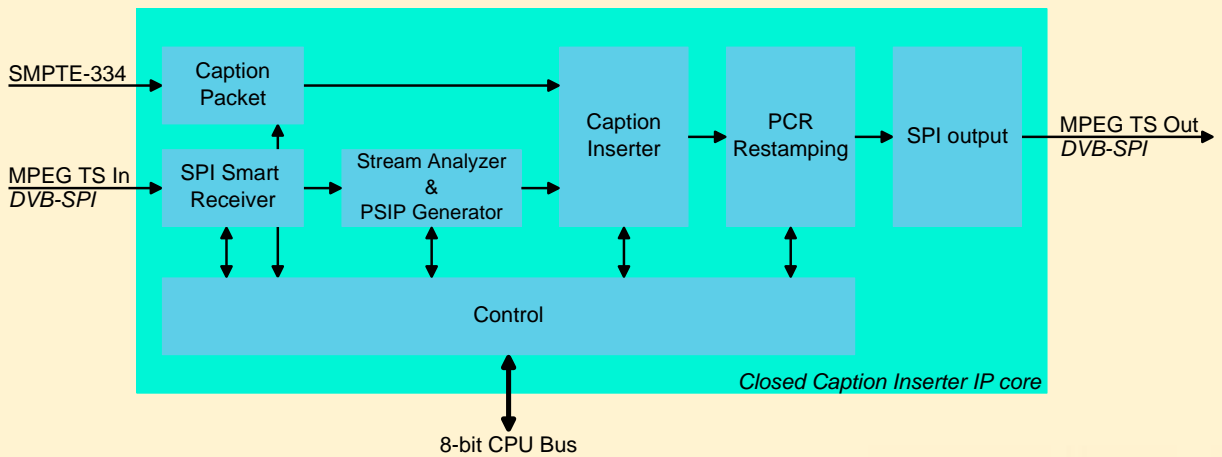- Ultrascale / Ultrascale +

MPEG-TS Processing

Closed Caption Inserter

Function

Insertion of DTV-708 closed caption into payload of MPEG video elementary stream

Applications

Can be used in addition to an MPEG encoder module to add specifics functionalities and make it consistent in regards of PSIP ATSC standard.

```
SMPTE-334 ──────▶ Caption Packet ──────────────────▶ Caption
                                                      Inserter ──▶ PCR
                                                                   Restamping ──▶ SPI output ──▶ MPEG TS Out
                                                                                                  DVB-SPI
MPEG TS In ──▶ SPI Smart ──▶ Stream Analyzer
DVB-SPI       Receiver       &
                             PSIP Generator

                              Control

                          8-bit CPU Bus
```

Closed Caption Inserter IP core

Main features

- 1 SPI input / 1 SPI output
- Insertion of DTV-708 closed caption into payload of MPEG video elementary stream

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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MPEG-TS Processing

UTC70

Function

Processing of multiple formatted input date/time to translate it into "Coordinated Universal Time" value with a reference starting from 1st of January 1970 at 00h00m00s.

Applications

Can be used with the MVD Remultiplexer Core to provide it reference time.
This reference time will then be automatically inserted in TDT/TOT or STT respectively for DVB or ATSC remultiplexer firmware.

GPS Rx →

GPS PPS In →

UTC70

→ PPS Out

→ UTC70 Out

NTP Interface ↔

UTC70 IP core

↕ 32-bit CPU Bus
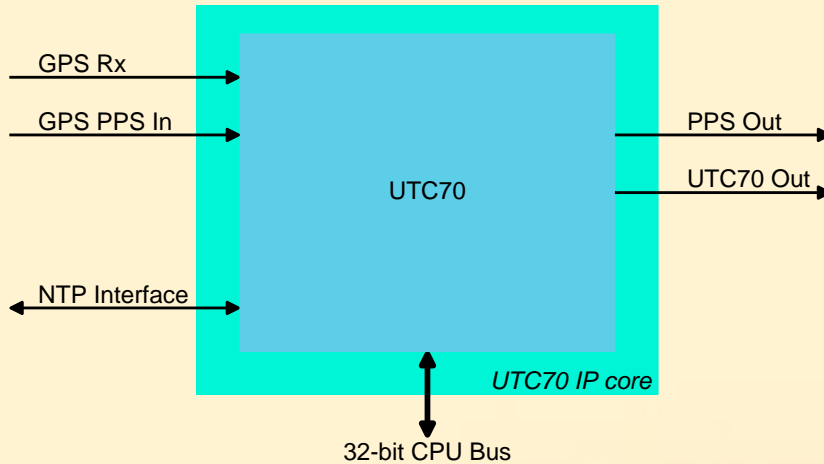
Main features

- 2 physical date/time input sources for automatic updating of the current date/time UTC value
- GPS interface is composed of
  • an UART RX line
  • a PPS input electrical line
  • GPRMC frame format from NMEA message
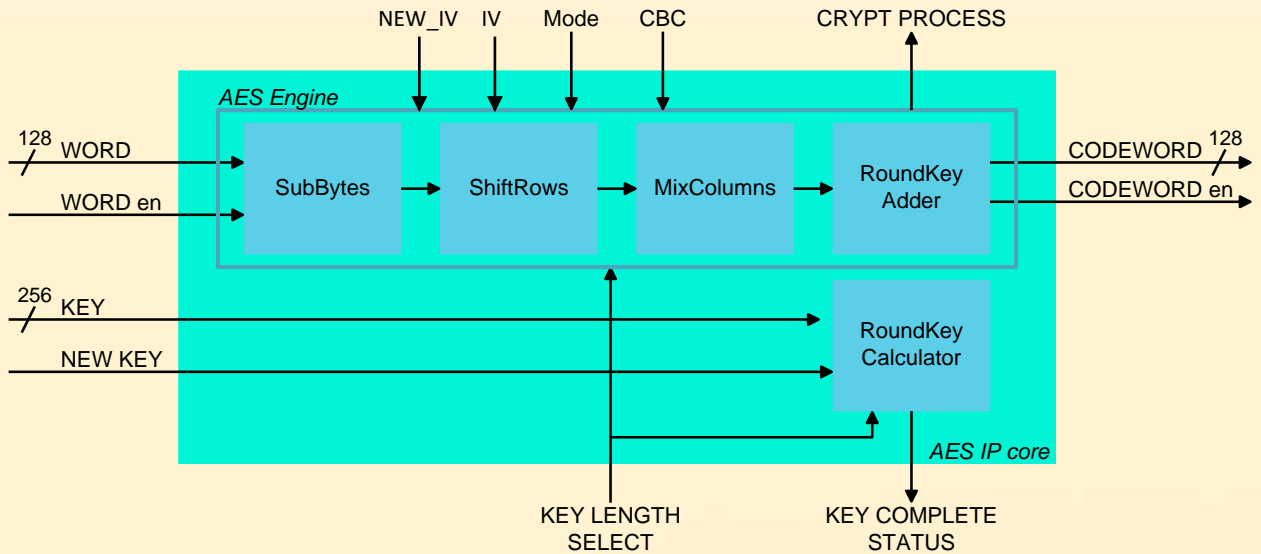- NTP interface

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

Encryption/Decryption

AES

Function	Applications
AES Encryption/Decryption	MPEG-TS stream encryption/ decryption, or any other encryption/decryption applications

| Main features	Supported Xilinx FPGAs
- 128/192/256-bit key size - ECB (Electronic Code Book) mode - CBC (Cipher Block Chaining) mode - Custom Init Vector (IV) for CBC mode	- Spartan-6, Virtex-6 - Virtex-7, Kintex-7, Artix-7 - Zynq - Ultrascale / Ultrascale +

Encryption/Decryption

MPEG-TS AES

Function

Encryption or decryption of MPEG-TS stream using the MVD AES encryption/ decryption core.

Applications

Can be used to encrypt MPEG-TS stream in order to broadcast it in a basic local network and gives access to the contents to only authorized user.
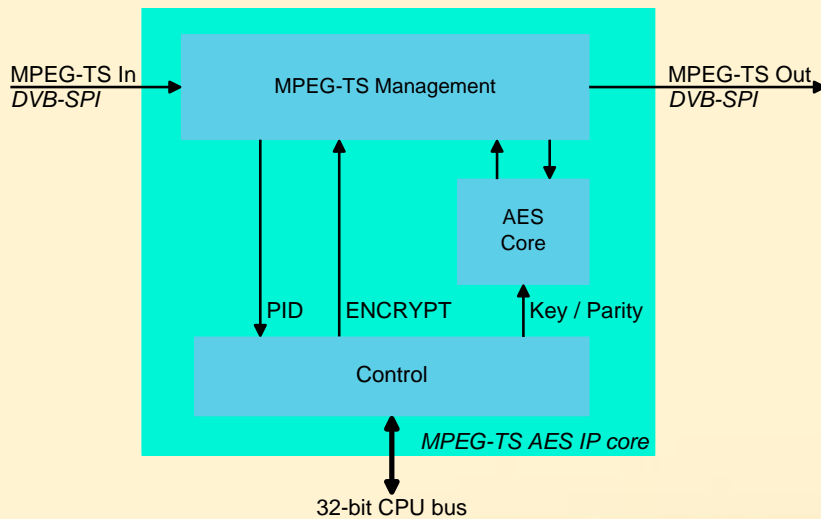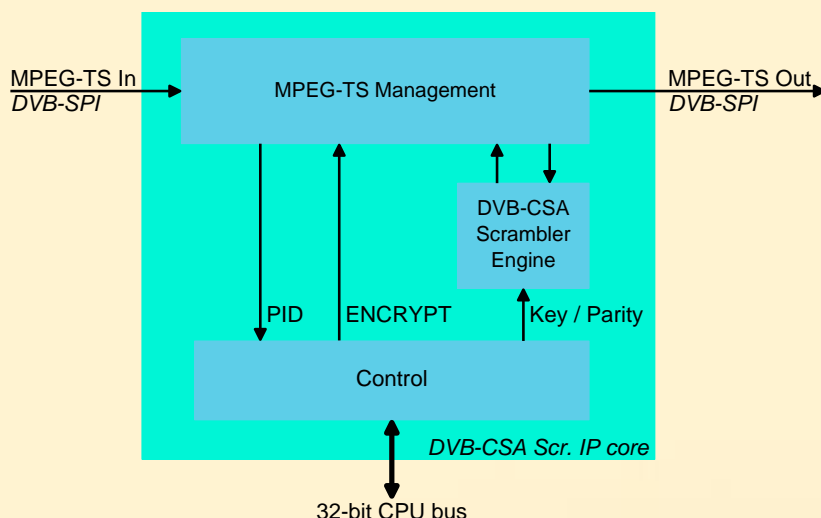

Main features

- Processes incoming stream and determines the packets that must be encrypted or decrypted according to the programmed configuration.
- The AES Interface module controls the AES core by sending it adapted Key and 128-bit Words to process.
- The module extracts words from MPEG TS interface and replaced them by AES processed words.
- Output packets are modified according to the process mode used.

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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DVB-CSA Scrambler

Function	Applications
Scrambling of MPEG-TS stream using ETSI specified DVB Common Scrambling Algorithm (CSA2)	MPEG-TS stream Scrambling, or any other encryption/decryption applications

Main features	Supported Xilinx FPGAs
- DVB/ATSC compliant - Manage odd/even key encryption - Selection of up to 64 PIDs and 32 Keys at the same time (any PID can use any key) - Automatically update encryption flags of MPEG-TS packet header - Supports 188, 204 and 208 bytes packet input - Supports Data Packet or Data Burst format - DVB-CSA Scrambler does not include ECM/EMM packets insertion nor CAT modification	- Spartan-6, Virtex-6 - Virtex-7, Kintex-7, Artix-7 - Zynq - Ultrascale / Ultrascale +

Important note

We are only able to license this IP core to customers that have signed the ETSI Non-Disclosure Agreement and are in possession of a valid license to use the Common Scrambling Algorithm. This is a requirement on all users of this technology, applied by the consortium who own the rights to the algorithm. Please feel free to contact MVD for more information on this requirement.
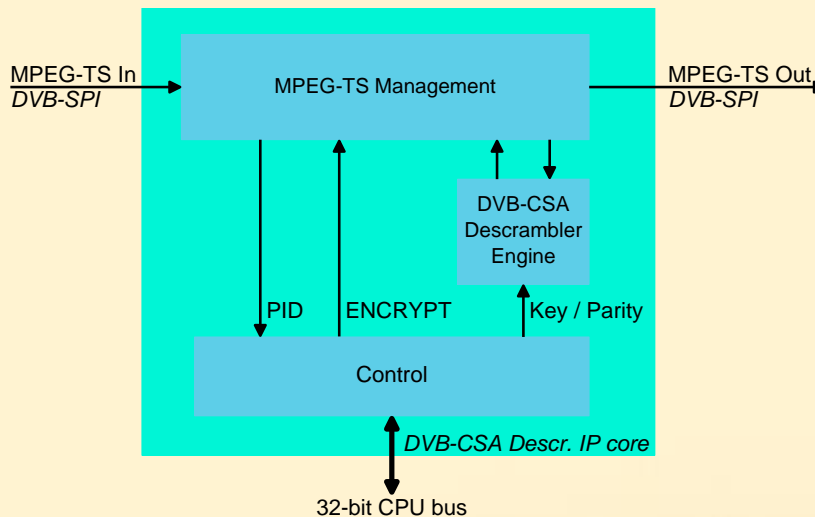
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Encryption/Decryption

DVB CSA®

DVB-CSA Descrambler

Function	Applications
Descrambling of MPEG-TS stream using ETSI specified DVB Common Scrambling Algorithm (CSA2)	MPEG-TS stream Descrambling, or any other encryption/decryption applications

Main features

- DVB/ATSC compliant
- Manage odd/even key encryption
- Selection of up to 64 PIDs and 32 Keys at the same time
  (any PID can use any key)
- Automatically update encryption flags of MPEG-TS packet header
- Supports 188, 204 and 208 bytes packet input
- Supports Data Packet or Data Burst format
- DVB-CSA Scrambler does not include ECM/EMM packets removing
  nor CAT modification

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

Important note

We are only able to license this IP core to customers that have signed the ETSI Non-Disclosure Agreement and are in possession of a valid license to use the Common Scrambling Algorithm. This is a requirement on all users of this technology, applied by the consortium who own the rights to the algorithm. Please feel free to contact MVD for more information on this requirement.

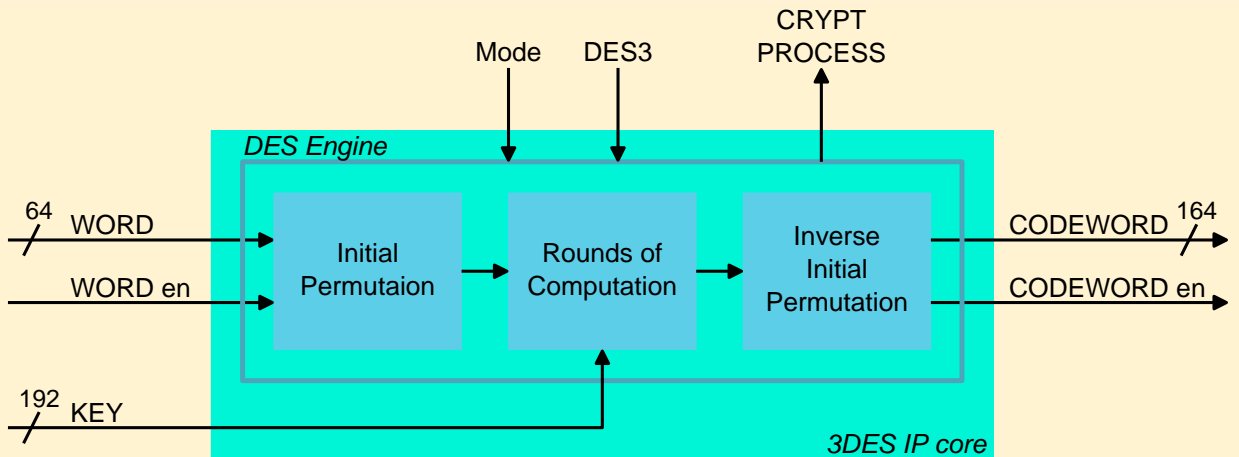MVD Cores – IP core solutions for Digital Video Broadcasting   V8- Rev A

Encryption/Decryption

3DES

Function	Applications
3DES encryption/decryption according to FIPS PUB 46-3	Applications related to MPEG-TS stream encryption, or any other encryption applications.

Main features

- Supports 192-bit key size
  (168-bit cipher key with 24 additional parity bits)
- Supports Single DES
- Key Parity Checking
- Same core can be used for encryption and decryption
- Automatic Roundkey generation inside the core
- ECB (Electronic Code Book) implementation per FIPS PUB 81

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
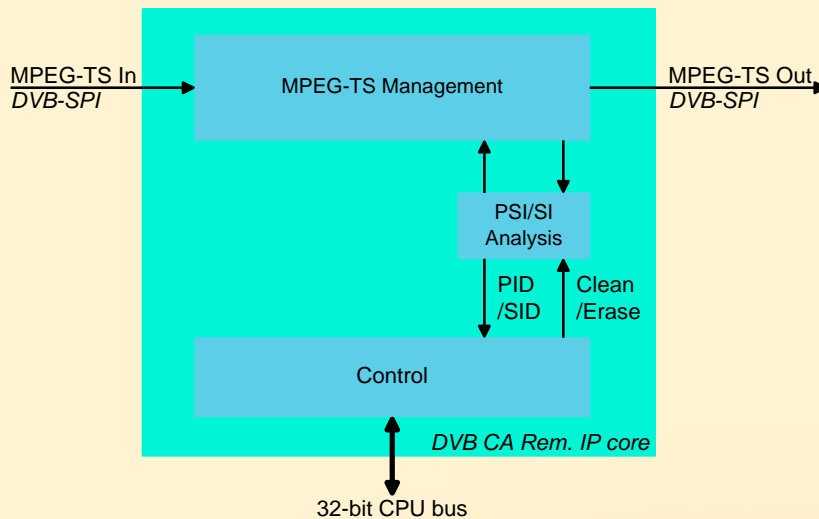- Ultrascale / Ultrascale +

Encryption/Decryption

DVB CA Remover

Function	Applications
Clearing of conditional access information from one or all services of an MPEG-TS stream	Clear one or all services of MPEG-TS stream in when the CA descrambler does not manage conditional access information but only payload decryption

MPEG-TS In *DVB-SPI* → **MPEG-TS Management** → MPEG-TS Out *DVB-SPI*

PSI/SI Analysis

PID/SID   Clean/Erase

Control

DVB CA Rem. IP core

32-bit CPU bus

Main features

- DVB compliant
- Auto adaptive and real time PSI/SI analysis and management
- Manage up to 124 services and all PID values
- Ability to filter CAT and associated EMM
- Remove PMT CA descriptor and associated ECM
- Erase CA Flag in SDT for the concerned services
- Erase CA Flag for all event in EIT for the concerned services
- Erase CA encryption bit in the packet header of the concerned elementary stream packets
- Regeneration of all CRC's tables
- Descrambling part is not ensured by DVB CA REMOVER but DVB-CSA Descrambling core

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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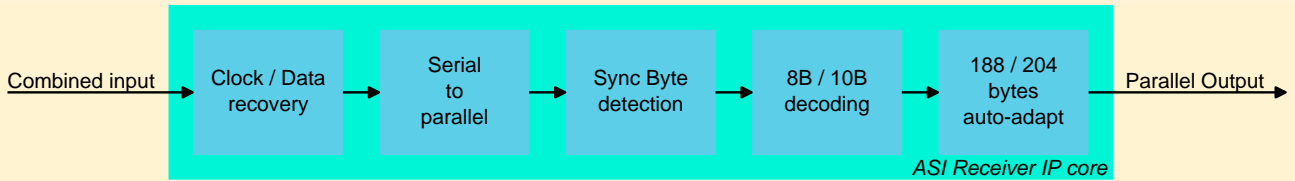
Interfaces

ASI Receiver

Function
Converts a DVB-ASI flow into a DVB-SPI flow according to EN500083-9 Annex B standard

Applications
DVB/MPEG-2 TS Serial / Parallel Conversion

Combined input → Clock / Data recovery → Serial to parallel → Sync Byte detection → 8B / 10B decoding → 188 / 204 bytes auto-adapt → Parallel Output

ASI Receiver IP core

Main features
- 27MHz Single Clock
- 188 or 204 bytes packet input
- Direct ASI interface (clock recovery from Data)
- Data Packet or Data Burst format

Supported Xilinx FPGAs
- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
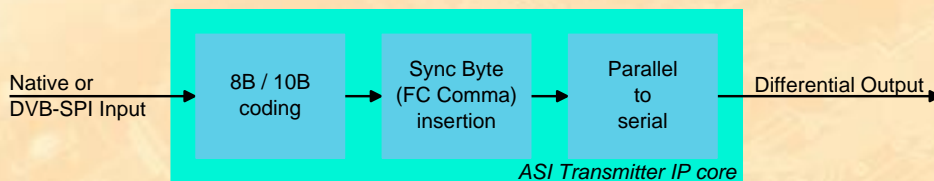- Zynq
- Ultrascale / Ultrascale +

ASI Transmitter

Function
Converts a DVB-SPI flow into a DVB-ASI flow according to EN500083-9 Annex B standard

Applications
DVB/MPEG-2 TS Parallel / Serial Conversion

Native or DVB-SPI Input → 8B / 10B coding → Sync Byte (FC Comma) insertion → Parallel to serial → Differential Output

ASI Transmitter IP core

Main features
- 135 MHz Single Clock
- 188 or 204 bytes packet input
- Data Packet or Data Burst format
- Choice of the output signal polarity

Supported Xilinx FPGAs
- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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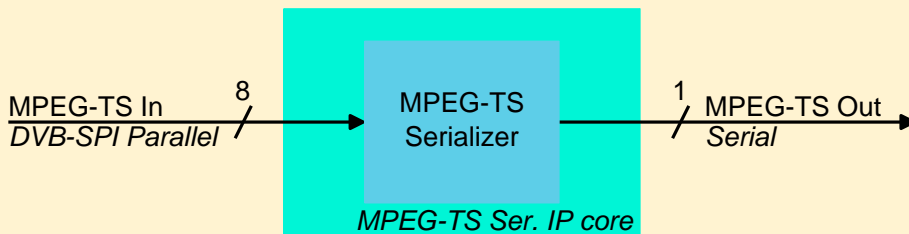
Interfaces

MPEG-TS Serializer

Function

Converts a parallel MPEG TS input stream into a serial MPEG TS output stream.

Applications

applications related to DVB/MPEG-TS transport streams for Serial Data transmission between FPGA.

MPEG-TS In *DVB-SPI Parallel* — 8 → **MPEG-TS Serializer** — 1 → MPEG-TS Out *Serial*

MPEG-TS Ser. IP core

Main features

- Incoming MPEG_TS clock resynchronization
- x47 sync signal recovery
- Parallel/Serial Conversion
- Auto adaptation to 188/204/208 bytes packet Input
- 188 bytes MPEG-TS serial output
- No coding mechanism

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
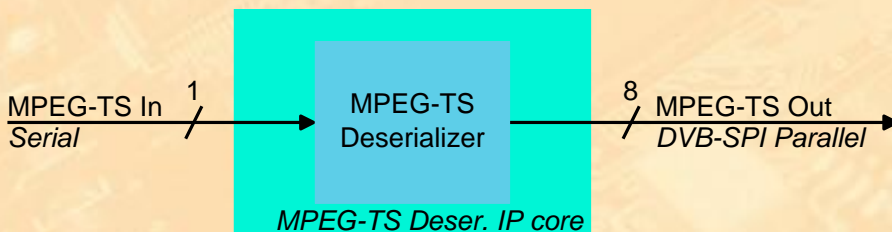- Zynq
- Ultrascale / Ultrascale +

MPEG-TS Deserializer

Function

Converts a serial MPEG TS input stream into a parallel MPEG TS output stream.

Applications

Applications related to DVB/MPEG transport streams for Satellite tuner data de-serialization.

MPEG-TS In *Serial* — 1 → **MPEG-TS Deserializer** — 8 → MPEG-TS Out *DVB-SPI Parallel*

MPEG-TS Deser. IP core

Main features

- Data acquisition on clock
- Serial/parallel Conversion
- Auto adaptation to 188/204 bytes packet Input
- 188 bytes MPEG-TS output
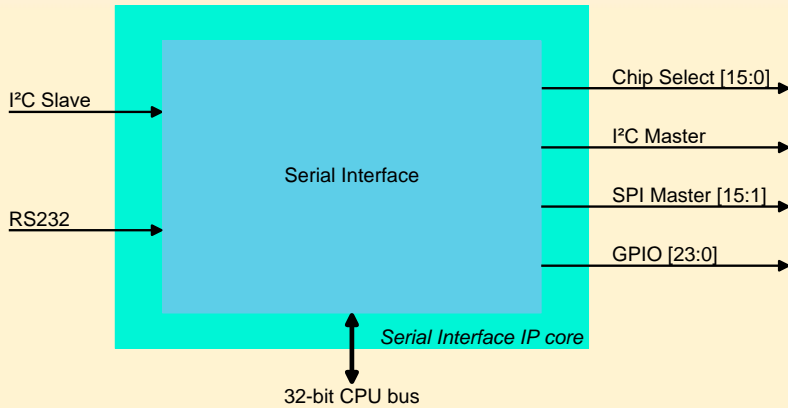- No decoding control

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

Interfaces

Serial Interface

Function

I²C/RS232 to 32-bit CPU bus interface

Applications

MVD IP cores initialization when no local CPU is available

Serial Interface IP core

Main features

Input can be:

- I2C 400KHz slave interface for 8-bit registers access
- UART interface with configurable Baud rates
 (from 9 600 to 921 600 Bauds), 8-bit, NO parity, 1 STOP bit

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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Interfaces

DDR User Interface for 7 Series

Function

Multiport interface between MCB (Spartan-6) and App UI (7 Series) interfaces of Xilinx MIG IP cores

Applications

The DDR User Interface IP core can be used when an IP core with MCB master ports needs to be connected to a Xilinx MIG for 7 Series
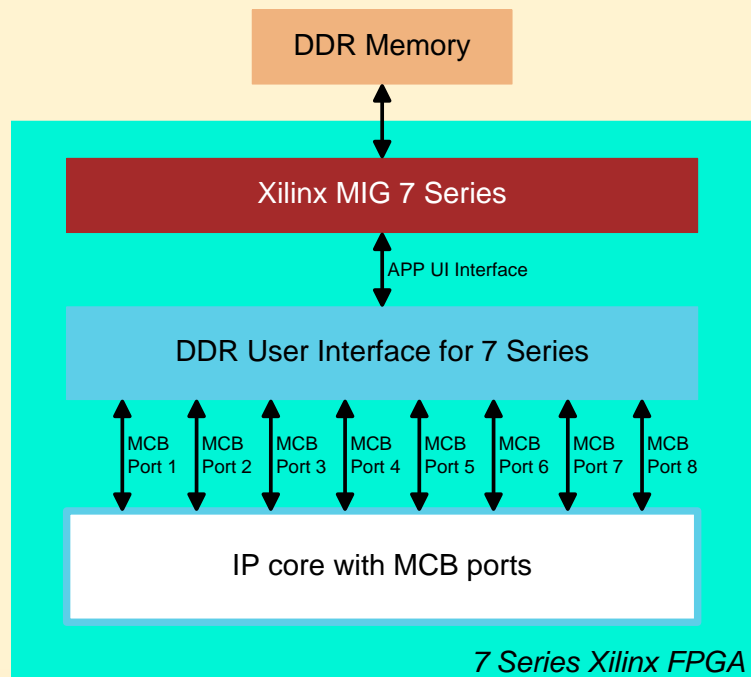
Main features

- 8 slave MCB interface portsUART interface
- 32 bits data MCB interface port only
- Bidirectional or unidirectional MCB interface port
- MCB interface ports clocks synchronous
  or asynchronous to global clock
- One User Interface master port for 16 bits DDR 4:1
  (Burst length at DDR memory is 8)

Supported Xilinx FPGAs

- Virtex-7, Kintex-7, Artix-7
- Zynq
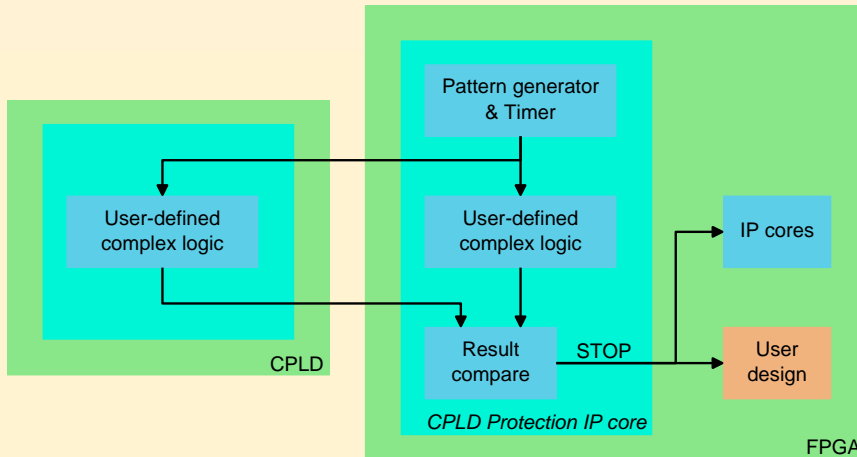- Ultrascale / Ultrascale +

Design Protection

CPLD

Function	Applications
Protection against FPGA bitstream copy.	Counterfeiting prevention

Main features

- External encrypted CPLD
- Source code of protection mechanism delivered
- Customer chooses its own codes for the protection

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
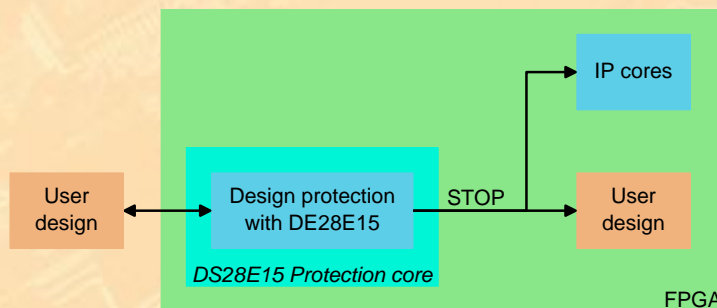- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

Maxim 1-wire DS28E15

Function	Applications
Protection against FPGA bitstream copy.	Counterfeiting prevention

Main features

- SH256 authentication through Maxim DS28E15 authenticator microchip
- 256-bits key size

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +
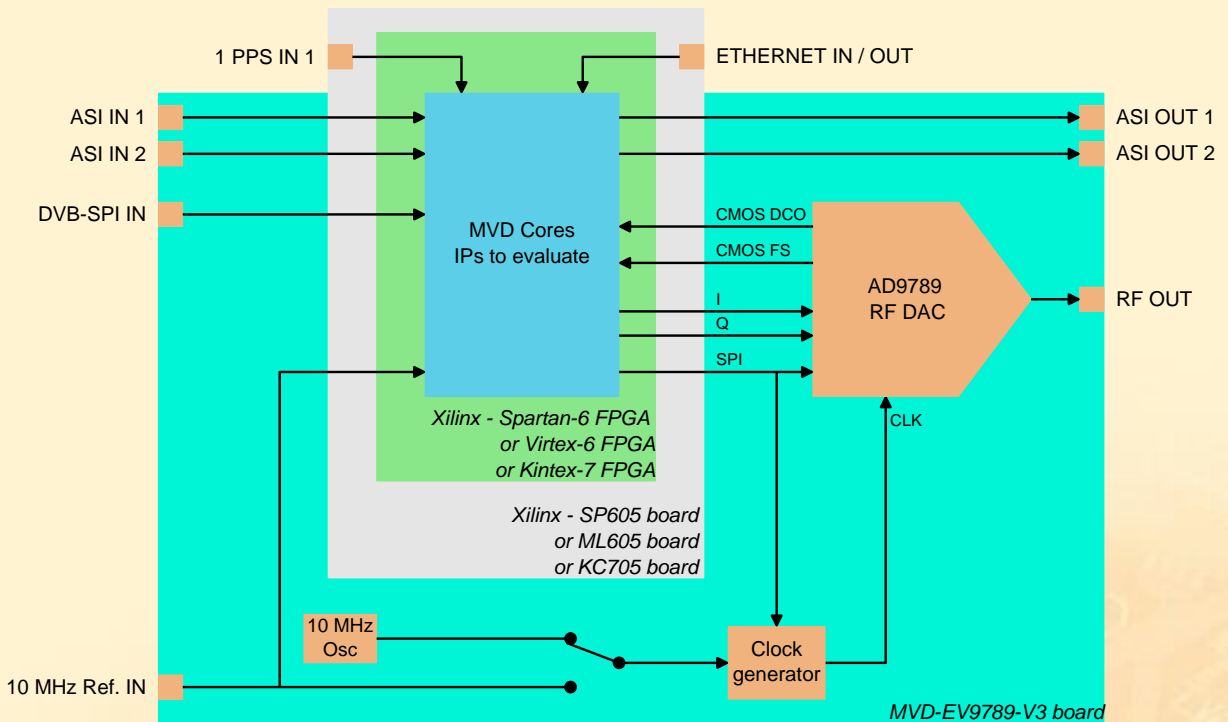
Evaluation board

MVD-EV9789-V3

Function

The MVD-EV9789-V3 board converts an MPEG TS stream into an RF signal and supports most of the digital TV standards (DVB-C, J.83B, DVB-T, ATSC, DVB-S, ..).

Applications

The MVD-EV9789-V3 board is a daughter board for the SP605/ML605/KC705 Xilinx evaluation boards. This pair of boards may be used for evaluation of MVD Cores' modulators / TS processing, IP cores or as a test equipment for demodulation devices.

Main features

- FMC connector to connect to Xilinx SP605 evaluation board
- 1 x USB input for cores configuration
- 1 x 10 MHz Clock Ref input
- 1 x 1PPS input
- 1 x SPI (Synchronous Parallel Interface) TS input
- 2 x ASI (Asynchronous Serial Interface) TS inputs
- 2 x ASI (Asynchronous Serial Interface) TS outputs
- 1 x MPEG TS over UDP/IP input/output
- 1 x IF/RF output (36 MHz to 1 GHz)
- "SFN Ready" for optional Single Frequency Networks

Supported Xilinx FPGAs

- Spartan-6, Virtex-6
- Virtex-7, Kintex-7, Artix-7
- Zynq
- Ultrascale / Ultrascale +

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Licensing

Our cores are sold at a fixed charge, royalty-free, independent of the production you can have.
There are two possible licenses: *Project License* or *Site License*.

With the *Project license* you can use our core for one specific project
(generally a project is defined by a model of printed circuit board).
For this given project, you can implement several instances of the same core.

With the *Site license*, you can use our core for all the projects developed at your "site".
Your "site" means a geographic location in which you conduct business, with a radius of no more than 5 miles.

Project license & Site license agreement templates are available on request.

Support

Remote technical support (by e-mail or phone) during 3 months from the first delivery is included in the prices above.

If needed, we can provide additional technical support (remote or on site).
Support can include FPGA pinout, assistance for your board schematics, DAC configuration, ...

If your company doesn't want to spend engineering resources regarding the FPGA implementation, and if there is no other logic than our IPs to integrate, we can also deliver the entire FPGA project and bitstream. Conditions will depend on the project.

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About MVD Cores

Company profile

MVD Cores is an engineering team highly specialized in Digital Video Broadcasting (DVB) and FPGA technologies.

We provide IP cores for Xilinx FPGAs dedicated to MPEG TS processing, transporting and modulation (DVB, J.83B, ATSC, IPTV standards).

The products and services catalog contains a wide range of on-the-shelf IPs to build solutions to carry MPEG-TS to RF.

Our IPs cover almost all worldwide standards of current technologies for broadcasting over Digital Terrestrial Television (DTT), Cable TV (CATV), Satellite and IPTV.

Our IPs are easy to implement and ready to use. MVD Cores can provide technical support during all the design phases and will help you to use all the benefits of the FPGA by carrying out modular solution and scalable architecture. The expertise field covers optimized DSP functions for modulation, SERDES, high speed functions implementa-tion, TS processing and System-On-Chip into the FPGA.

Our cores have been tailored to meet the requirements of most applications while using the lowest cost compo-nents and the lower amount of resources. However they can be adapted to specific needs.

MVD's cores enable its customers to build their high-end products while speeding up development phases.

Partners

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ALLIANCE PROGRAM
MEMBER

MVD Cores is a Member of the **Xilinx Alliance Program**

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