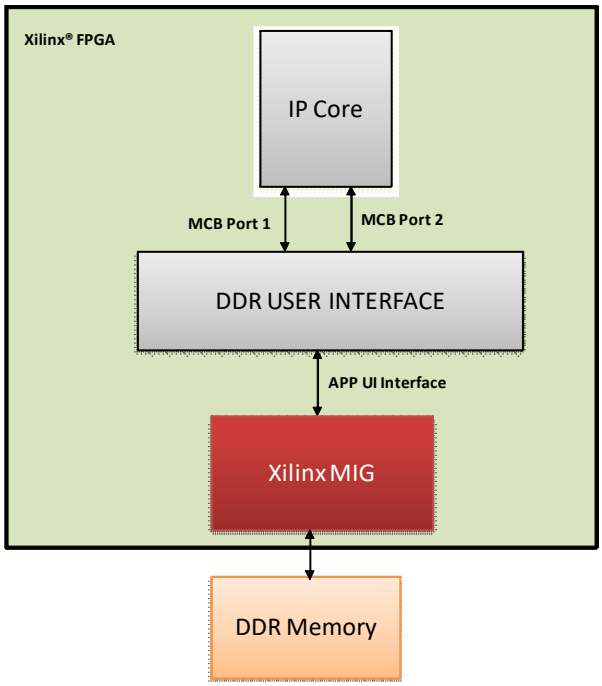
DDR USER INTERFACE V4.0

Product Brief (October 2019 - Rev A)

Features

This core provides an interface between the two generations of Xilinx MIG IP core.

- **Drop-in module for, Artix-7™, Kintex-7™, Virtex-7™ FPGAs, Zynq™ and later FPGA**
- **8 slave MCB interface ports**
- **32 bits data MCB interface port only**
- **Bidirectional or unidirectional MCB interface port**
- **MCB interface ports clocks synchronous or asynchronous to global clock**
- **One User Interface master port for 16 bits DDR 4:1 (Burst length at DDR memory is 8)**
- **Fully synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Applications

The DDR User Interface IP core can be used when an IP core with MCB master ports needs to be connected to a Xilinx MIG (7 Series or Later).

Resource Estimation

Resources utilization depends on user interface size (linked to DDR size), number of MCB ports and synchronous or asynchronous interfaces.

The maximal configuration requires:

	Slices	LUTs	BRAMs (18k)
7 Series	**3 750**	**9 500**	**16**

Ordering information and related cores

Parameters	Designation
n Slave MCB PORTS	**MVD_DDR_USER_INTERFACE_nP_NET**

n from 1 to 8

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: Core DVB-T2, Core RTP RX/TX, Core Remultiplexer, Core DDR MUX
Contact us at *info_cores@mvd-fpga.com*

Documentation and support: Datasheet and user's guide. In addition MVD can provide on site or remote coaching.