

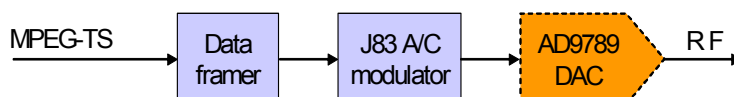


### Features

ITU-T J.83 Annex A/C, DVB-C (ETS 300 429)  
 Compliant baseband transmitter for Cable Modem Termination Systems (CMTS)

- The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)
- Drop-in module for Virtex-6™, Virtex-5™, Virtex-4™, Spartan-6™ and Spartan™-3/E/A FPGAs
- Single clock (up to 140 MHz+ for Spartan-3/6™, 180 MHz+ for Virtex-4/5/6™)
- Robust SPI input (discarding incorrect input packets)
- PCR re-stamping
- Supports programmable symbol rates
- Programmable 16, 32, 64, 128 and 256 QAM Symbol Mapping
- Complex baseband outputs (2 x 8 bits)
- Single / multi channel
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 42dB

Complete application fits into 3S50A and/or 3S100E depending on selected options



### Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation
Spartan3/E/A	700	3	1	2	
Spartan 6	450	3	1	2	
Virtex 4	650	3	1	2	
Virtex 5	450	3	1	2	
Virtex 6	350	3	1	2	

*(values may vary depending on implementation options)*

## **Ordering information and related cores**

<b>Parameters</b>	<b>Designation</b>
Fixed	<b>MVD_DVBC_J83AC_AD9789_FIXED_NET</b>
GPIO programmable	<b>MVD_DVBC_J83AC_AD9789_GPIO_NET</b>
CPU programmable	<b>MVD_DVBC_J83AC_AD9789_CPU_NET</b>

**VHDL source code** : can be delivered as an option under NDA and other specific clauses

**Complementary cores** : DVB-C for IF output, Upconverter for AD9739 DAC or MAX5881 DAC, contact us. For a multi-channel application, we recommend to use the AD9789 for 4 adjacent channels, or we recommend to use the AD9739 DAC or the MAX5881 DAC for more than 4 channels, or for non adjacent channels.

**Related cores** : Cable Modulator J83B, DVB-S, DVB-T/H, DVB Remultiplexer and/or ASI Receiver cores contact us at [info\\_cores@mvd-fpga.com](mailto:info_cores@mvd-fpga.com)

**Documentation and support** : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.