



Features

DVB-S (ETS 300 421)

Compliant baseband transmitter for Satellite Modem Termination Systems (SMTS)

- The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)
- Drop-in module for Virtex-6™, Virtex-5™, Spartan-6™ and Spartan™-3/E/A FPGAs
- Single clock (up to 140 MHz+ for Spartan-3/6™, 180 MHz+ for Virtex-5/6™)
- Robust SPI input (discarding incorrect input packets)
- PCR re-stamping
- Supports programmable symbol rates
- Programmable 1/2, 2/3, 3/4, 5/6 and 7/8 punctured FEC
- Baseband or Intermediate frequency output for complex DAC (2 x 16 bits)
- Single / multi channel
- Fully synthesisable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 40dB

Complete application fits into 3S500E and/or 3S400A depending on selected options



Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables : - Datasheet - Netlist for core generation
Spartan-3/E/A	3 150	3	20	2	
Spartan-6	1 350	3	16	2	
Virtex-5	1 550	3	16	2	
Virtex-6	1 250	3	16	2	

(values may vary depending on implementation options)

Ordering information and related cores

Parameters	Designation
Fixed	MVD_DVBS_FIXED_NET
GPIO programmable	MVD_DVBS_GPIO_NET
CPU programmable	MVD_DVBS_CPU_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Complementary cores : DVB-S for AD9789 DAC, Upconverter for AD9739 DAC or MAX5881 DAC, contact us. For a multi-channel application, we recommend to use the AD9739 DAC or the MAX5881 DAC.

Related cores : Cable Modulator J83B, DVB-C, DVB-T/H, DVB Remultiplexer and/or ASI Receiver/Transmitter cores, contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet. In addition MVD can provide on site or remote coaching.