DVB-S Modulator Core V3.0

Product Brief (March 2009 - Rev A)

Features

DVB-S (ETS 300 421)
Compliant baseband transmitter for Satellite Modem Termination Systems (SMTS)

- **Drop-in module for Virtex-5™, Virtex-4™ and Spartan™-3/E/A FPGAs**
- **Single clock (up to 140 MHz+ for Spartan-3™, 180 MHz+ for Virtex-4™ and Virtex-5™)**
- **Robust SPI input (discarding of incorrect input packets)**
- **PCR re-stamping**
- **Supports programmable symbol rates**
- **Programmable 1/2, 2/3, 3/4, 5/6 and 7/8 punctured FEC**
- **Intermediate frequency output for single DAC (14 bits) or complex DAC (2 x 16 bits)**
- **Single channel – support for multi channel**
- **Full synthetizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**
- **MER > 40dB**

Complete application fits into 3S500E and/or 3S400A depending on selected options

Applications

DVB-S may be used in applications related to satellite transmission.

Description

The MVD DVB-S core is a drop-in module that includes the following functions :

- **Input data framer from DVB-SPI source (MPEG-TS flow)**
- **DVB-S modulator (Energy dispersal, Reed-Solomon encoder, interleaver, convolutional encoder and puncturing)**
- **RRC filter**
- **Flexible Digital Up Converter**
- **Modulator for IF output**
- **Output for simple DAC (14 bits) or complex DAC (2x16bits)**

Companion cores

- **ASI receiver core**
- **DVB remultiplexer core**
- **Adaptive MPEG-TS data rate core**
- **Serial Interface for CPU configuration**

Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface.

	Slices	BRAMs	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation
Spartan3/E/A	**3 000**	**5**	**16**	**2**	
Virtex 4	**2 800**	**5**	**16**	**2**	
Virtex 5	**1 450**	**3**	**16**	**2**	
(values may vary depending on implementation options)					

Ordering information and related cores

Parameters	Designation
Fixed	**MVD_DVBS_FIXED_NET**
GPIO programmable	**MVD_DVBS_GPIO_NET**
CPU programmable	**MVD_DVBS_CPU_NET**

VHDL source code : can be delivered as an option under NDA and other specific clauses
Related cores : Cable Modulator J83B, J83B 4-Channel, DVB-C, DVB-T/H, DVB Remultiplexer and/or ASI Receiver cores, contact us at *info_cores@mvd-fpga.com*
Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.

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