### Features
ETSI, DVB-T/H (EN 300 744 V1.5.1) Compliant baseband transmitter for Digital Terrestrial Television

- The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)
- Drop-in module for Spartan-6™, Virtex-6™, Artix-7™, Kintex-7™ and Virtex-7™ FPGAs
- Single clock (up to 150 MHz)
- Robust SPI input (discarding incorrect input packets)
- PCR re-stamping
- Single channel, supports hierarchical transmission
- Configurable Convolutional Rate
- Configurable in-depth interleaving for DVB-H
- Programmable QPSK, 16-QAM and 64-QAM Symbol Mapping
- Configurable support for 2k, 8k and 4k (DVB-H) OFDM modes
- Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)
- Supports variable channel width 5MHz to 8MHz
- Intermediate frequency output for single DAC (14 bits) or baseband outputs (2 x 16 bits)
- Single / multi channel
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 42dB
- Carrier Suppression > 45dB

### Applications
The MVD DVB-T/H modulator may be used in applications related to terrestrial transmission, typically at the head end.

### Description
The MVD DVB-T/H modulator is a drop-in module that includes the following functions:

- Input data framer from DVB-SPI source (MPEG-TS flow)
- DVB-T/H modulator (Energy dispersal, Reed Solomon encoder, Convolutional interleaver, FEC convolution encoder, Inner interleaver, QPSK/QAM symbol mapper, Framer with pilots & TPS inserter, IFFT and guard interval insertion)
- Flexible Digital Upsampler
- Modulator for IF output
- Output for simple DAC (14 bits) or baseband outputs (2x16bits)

### Companion cores
- ASI receiver core
- DVB remultiplexer core
- Serial Interface for CPU configuration
- I2C Slave Interface core
**Resource Utilization**

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface and without hierarchical transmission option.

<table>
<thead>
<tr>
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<th>Slices</th>
<th>LUTs</th>
<th>BRAMs (18k)</th>
<th>Mults/DSP48</th>
<th>BUFG</th>
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**Deliverables:**
- Datasheet
- Netlist for core generation

**Ordering information and related cores**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Designation</th>
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<tbody>
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<td>MVD_DVBTH_FIXED_NET</td>
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<tr>
<td>CPU programmable</td>
<td>MVD_DVBTH_CPU_NET</td>
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<tr>
<td>CPU programmable + Hierarchy</td>
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**VHDL source code:** can be delivered as an option under NDA and other specific clauses

**Complementary cores:** DVB-T/H for AD9789 DAC, Upconverter for AD9739 DAC or MAX5881 DAC, contact us.
For a multi-channel application, we recommend to use the AD9789 for 4 adjacent channels, or we recommend to use the AD9739 DAC or the MAX5881 DAC for more than 4 channels, or for non adjacent channels.

**Related cores:** Cable Modulator J83B, DVB-S, DVB-C, DVB Remultiplexer and/or ASI Receiver cores contact us at info_cores@mvd-fpga.com

**Documentation and support:** Datasheet and user’s guide. In addition MVD can provide on site or remote coaching.