

Features

ETSI, DVB-T/H (EN 300 744 V1.5.1)
Compliant baseband transmitter for Digital Terrestrial Television

- The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)
- Drop-in module for Virtex-6™, Virtex-5™, Spartan-6™ and Spartan™-3/E/A FPGAs
- Single clock (up to 140 MHz+ for Spartan-3/6™, 180 MHz+ for Virtex-5/6™)
- Robust SPI input (null packet deletion in option)
- PCR re-stamping
- Single channel, supports hierarchical transmission
- Configurable Convolutional Rate
- Configurable in-depth interleaving for DVB-H
- Programmable QPSK, 16-QAM and 64-QAM Symbol Mapping
- Configurable support for 2k, 8k and 4k (DVB-H) OFDM modes
- Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)
- Supports variable channel width 5MHz to 8MHz
- Complex base band output (2 x 16 bits)
- Single / multi channel
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 42dB
- Carrier Suppression > 45dB

Applications

The MVD DVB-T/H modulator may be used in applications related to terrestrial transmission, typically at the head end.

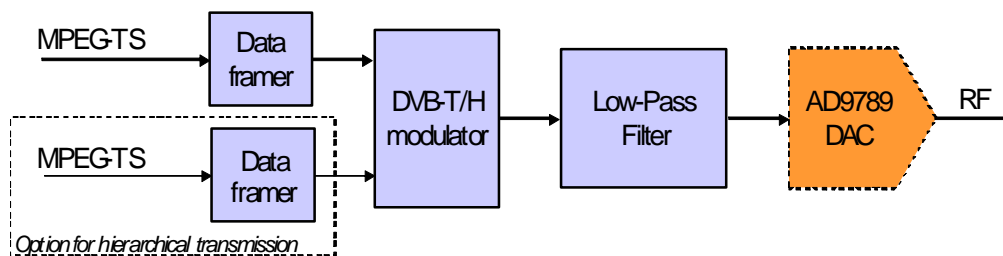
Description

The MVD DVB-T/H modulator is a drop-in module that includes the following functions :

- Input data framer from DVB-SPI source (MPEG-TS flow)
- DVB-T/H modulator (Energy dispersal, Reed Solomon encoder, Convolutional interleaver, FEC convolution encoder, Inner interleaver, QPSK/QAM symbol mapper, Framers with pilots & TPS inserter, IFFT and guard interval insertion)
- Low Pass Filter
- Output for complex DAC (2x16bits)

Companion cores

- ASI receiver core
- DVB remultiplexer core
- Serial Interface for CPU configuration
- I2C slave Interface core



Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface and without hierarchical transmission option.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables : - Datasheet - Netlist for core generation
Spartan-3/E/A	3 100	41	13	2	
Spartan-6	1 200	43	11	2	
Virtex-5	1 500	41	13	2	
Virtex-6	1 200	41	11	2	
<i>(values may vary depending on implementation options)</i>					

Ordering information and related cores

Parameters	Designation
CPU programmable	MVD_DVBTH_AD9789_CPU_NET
CPU programmable + Hierarchy	MVD_DVBTH_AD9789_CPU_HIERARCHY_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Complementary cores : DVB-T/H for IF output, Upconverter for AD9739 DAC or MAX5881 DAC, contact us. For a multi-channel application, we recommend to use the AD9789 for 4 adjacent channels, or we recommend to use the AD9739 DAC or the MAX5881 DAC for more than 4 channels, or for non adjacent channels.

Related cores : Cable Modulator J83B, DVB-S, DVB-C, DVB Remultiplexer and/or ASI Receiver/Transmitter cores contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet. In addition MVD can provide on site or remote coaching.