

Features

ETSI, DVB-T/H (EN 300 744 V1.5.1)
Compliant baseband transmitter for Digital Terrestrial Television

- Drop-in module for Virtex-5™, Virtex-4™ and Spartan™-3 FPGAs
- Single clock (up to 140 MHz+ for Spartan-3™, 160 MHz+ for Virtex-4™ and 180 MHz+ for Virtex-5™)
- Robust SPI input (discarding of incorrect input packets)
- PCR re-stamping
- Single channel, supports hierarchical transmission
- Configurable Convolutional Rate
- Configurable in-depth interleaving for DVB-H
- Programmable QPSK, 16-QAM and 64-QAM Symbol Mapping
- Configurable support for 2k, 8k and 4k (DVB-H) OFDM modes
- Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)
- Supports variable channel width 5MHz to 8MHz
- Intermediate frequency output for single DAC (14 bits) or complex DAC (2 x 16 bits)
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 40dB
- Carrier Suppression > 45dB

Applications

The MVD DVB-T/H modulator may be used in applications related to terrestrial transmission, typically at the head end.

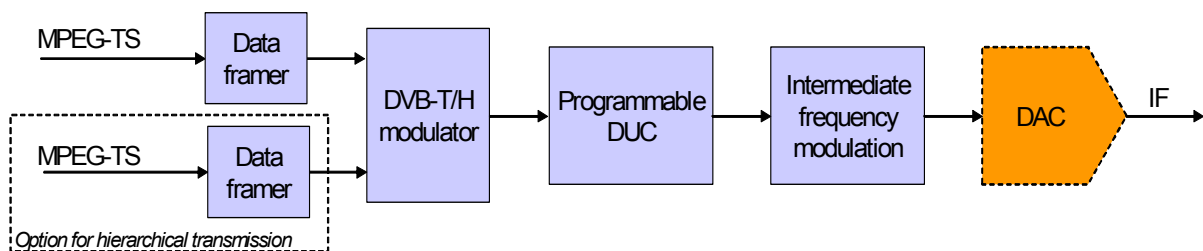
Description

The MVD DVB-T/H modulator is a drop-in module that includes the following functions :

- Input data framer from DVB-SPI source (MPEG-TS flow)
- DVB-T/H modulator (Energy dispersal, Reed Solomon encoder, Convolutional interleaver, FEC convolution encoder, Inner interleaver, QPSK/QAM symbol mapper, Framers with pilots & TPS inserter, IFFT and guard interval insertion)
- Flexible Digital Up Converter
- Modulator for FI output
- Output for simple DAC (14 bits) or complex DAC (2x16bits)

Companion cores

- ASI receiver core
- DVB remultiplexer core
- Adaptive MPEG-TS data rate core
- Serial Interface for CPU configuration



Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface and without hierarchical transmission option.

	Slices	BRAMs	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation
Spartan 3™	5 350	43	24	2	
Virtex 4™	4 850	43	26	2	
Virtex 5™	2 350	22	26	2	

(values may vary depending on implementation options)

Ordering information and related cores

Parameters	Designation
Fixed	MVD_DVBTH_FIXED_NET
CPU programmable	MVD_DVBTH_CPU_NET
CPU programmable + Hierarchy	MVD_DVBTH_CPU_HIERARCHY_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : Cable Modulator J83B, DVB-S, DVB-C, DVB Remultiplexer and/or ASI Receiver cores

contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.