ISDB-T Modulator Core V3.0

Product Brief (September 2019 – rev A)

Features

ARIB STD-B31 compliant modulator.

- **The MVD ISDB-T modulator core is delivered for baseband output to be natively connected to AD9789 DAC from Analog Devices but can be used in Intermediate Frequency application (for Analog Devices (AD9744)) or in RF application when respectively connected to our UPSAMPLER or our UPCONVERTER core (for Analog Devices (AD9739A) or Maxim RF DACs (MAX5881)).**
- **Drop-in module for 6 Series, 7 Series and later Xilinx FPGAs**
- **Dual clock (CLK,CLKx2), CLK frequency equal to DAC clock frequency (up to 160 MHz)**
- **Single external memory (DDR memory)**
- **TS input only (one by layer)**
- **Robust SPI input (discarding incorrect input packets)**
- **PCR re-stamping**
- **3-Layer (A,B and C) modulator**
- **Configurable Convolutional Rate**
- **Programmable DQPSK, QPSK, 16-QAM and 64-QAM Symbol Mapping**
- **Configurable support for 2k, 4k and 8k OFDM modes (modes 1, 2 & 3)**
- **Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)**
- **Time Interleaving (length from 0 to 16)**
- **Supports variable channel width 6MHz to 8MHz**
- **Full 13-segment ISDB-T modulator**
- **Complex baseband outputs (2 x 16 bits) @ Fsymbol rate**
- **Fully synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**
- **MER > 42dB**

Applications

ISDB-T modulator IP may be used in applications related to terrestrial transmission, typically at the head end.

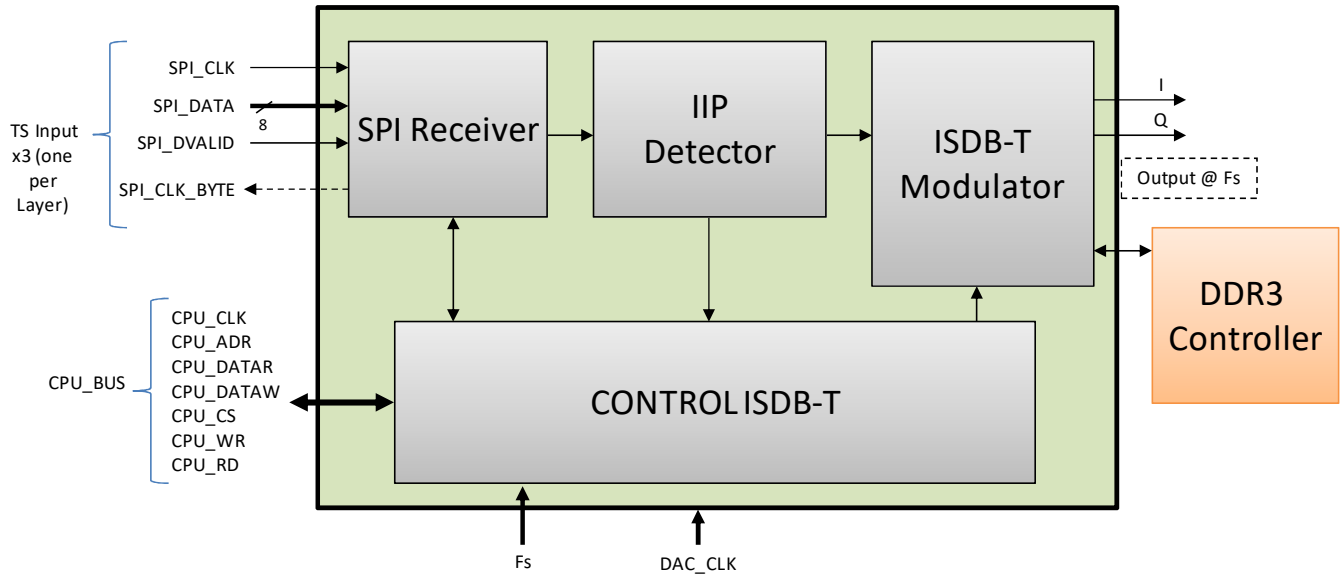
Description

The MVD ISDB-T core is a drop-in module that includes the following functions :

- **Input data framer from DVB-SPI source (MPEG-TS flow)**
- **ISDB-T modulator (Reed-Solomon encoder, Energy dispersal, Convolutional interleaver, FEC convolution encoder, QAM symbol mapper, Time & Frequency Interleaver, IFFT)**
- **Low Pass Filter**
- **Output for complex DAC (2 x 16 bits)**

Companion cores

- **ASI receiver core**
- **DVB remultiplexer core**
- **Serial Interface for CPU configuration**
- **I2C Slave Interface core**



Resource Utilization

	Slices	LUTs	BRAMs (18k)	Mults/DSP48
6-Series	**4100**	**11200**	**82**	**34**
7-Series	**4000**	**11200**	**85**	**26**

Ordering information and related cores

Version	Designation
Single layer	**MVD_ISDBT_ONE_LAYER_TS_CPU_NET**
3-layer	**MVD_ISDBT_THREE_LAYER_TS_CPU_NET**

VHDL source code: Can be delivered as an option under NDA and other specific clauses.

Related cores: Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB-T2, DVB Remultiplexer and/or ASI interface cores, contact us.

Documentation and support: Datasheet and user's guide. In addition MVD can provide on site or remote coaching.