MCB Port Multiplexer N to 1 Core V3.0

Product Brief (July 2019 - Rev A)

Description

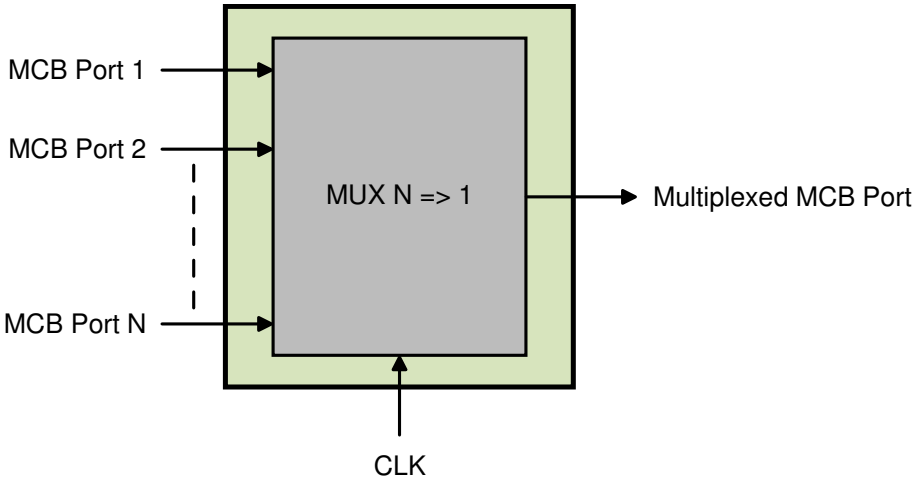
MVD Cores develops IP cores which need DDR External Memory. To spare resources or to allow more components to have access to DDR memory MVD has designed MCB interfaces ports Multiplexer N to 1 for Xilinx® components.

Applications

The MCB port Multiplexer IP core can be used to extend the number of MCB interfaces or to reduce implementation resources.

Features

- **Drop-in module for, 7 Series and later Xilinx FPGAs**
- **8 MCB input interface ports (each channel can be trimmed during implementation process)**
- **Can support unidirectional and bidirectional**
- **1 MCB output interface which time multiplexed the inputs**
- **32 bits data MCB interface port only**
- **Fully synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Resource Estimation

For 8 Channels Read/Write implemtented (i.e ACTIVATE_CHANNEL_i driven to VCC)

	Slices	LUTs	BRAMs (18k)
Spartan-6	**580**	**2200**	**0**
7 Series	**580**	**2200**	**0**

Ordering information and related cores

Parameters	Designation
None	**MVD_DDR_MUX _NET**

VHDL source code: can be delivered as an option under NDA and other specific clauses

Documentation and support: Datasheet and user's guide. In addition MVD can provide on site or remote coaching.