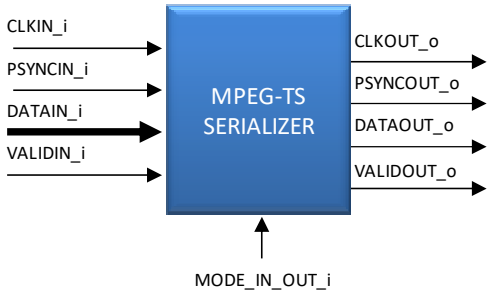
MPEG-TS_SERIALIZER Core V2.0

Product Brief (April 2015 - Rev A)

Features

Parallel MPEG_TS input stream to Serial MPEG-TS output Stream converter

- **Drop-in module for Spartan-3™, Spartan-6™, 7-Series™ FPGAs**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Applications

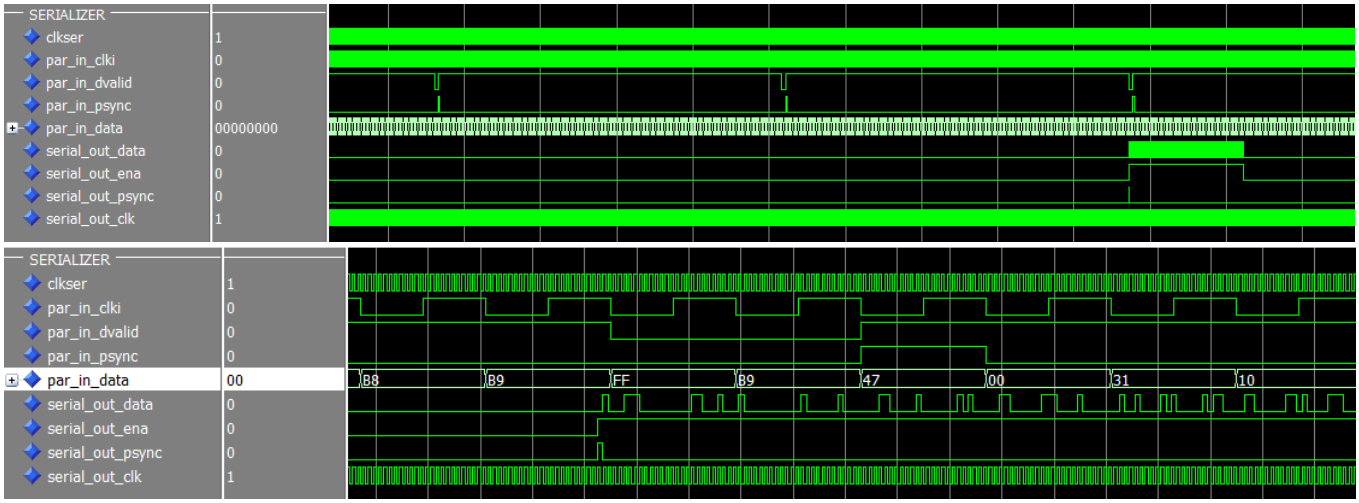
MVD MPEG-TS_SERIALIZER may be used in applications related to DVB/MPEG-TS transport streams for Serial Data transmission between FPGA.

Description

The MVD MPEG-TS_SERIALIZER core is a drop-in module that includes the following functions :

- **Incoming MPEG_TS clock resynchronization**
- **x47 sync signal recovery**
- **Parallel/Serial Conversion**
- **Auto adaptation to 188/204/208 bytes packet Input**
- **188 bytes MPEG-TS serial output**
- **No coding mechanism**
- **Rising/edge input/output configurable**

Rising / falling edge are controlled by *MODE_IN_OUT_i* : bit 0 = input ; bit 1 = output. (0 = rising ; 1 = falling).



Resource Utilization

The core configuration may be set by conditional synthesis .

	Slices (LUTs)	BRAMs (18k)	DDR_IO	BUFG
Spartan-3	**282 (503)**	**0**	**1**	**1**
Series-6	**62 (171)**	**0**	**1**	**1**
Series-7	**79 (172)**	**0**	**1**	**1**

Deliverables :

- **Netlist for core generation**

Ordering information and related cores

Designation
MVD_MPEG-TS_SERIALIZER_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses
Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Transmitter cores, contact us at *info_cores@mvd-fpga.com*