MPEG-TS AES CORE v1.0

Product Brief (February 2017 - Rev A)

Description

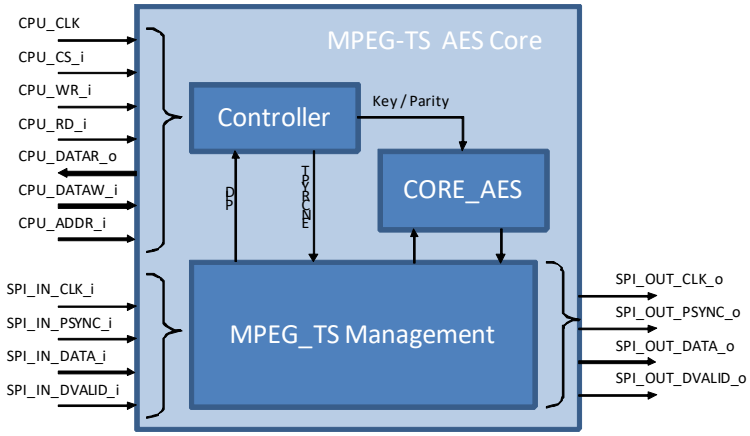
- **MPEG-TS AES core allows to encrypt or decrypt MPEG-TS stream using the native MVD AES encryption core**
- **The MPEG-TS AES core processes the incoming stream and determines the packets that must be encrypted or decrypted according to the programmed configuration.**
- **The MPEG-TS AES core controls the AES module by sending it adapted Key and 128-bit Words to process.**
- **The module extracts words from MPEG TS interface and replaced them by AES processed words.**
- **Output packets are modified according to the process mode used.**

Applications

- **The MPEG-TS AES core can be used to encrypt MPEG-TS stream in order to broadcast it in a basic local network and gives access to the contents to only authorized user.**

Features

- **Drop-in module for Spartan™-6, Virtex™-6, Artix™-7, Kintex™-7 and Virtex™-7 FPGAs**
- **IS0-13818-1 MPEG stream compliant**
- **DVB/ATSC/ISDB compliant**
- **Manage odd/even key encryption**
- **Selection of Encryption Key Size between 128, 192 and 256 bits**
- **Selection of any 8192 possibles PIDs(user must take care not to encrypt PSI/SI or PSIP tables)**
- **Automatically update encryption flags of MPEG-TS packet header**
- **Supports 188, 204 and 208 bytes packet input**
- **Supports Data Packet or Data Burst format**
- **MPEG-TS AES core does not include ECM/EMM packets insertion nor CAT modification (see remultiplexer core option for these features)**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Resource Utilization (AES Core included)

	Slices	LUTs	BRAMs (18k)	DSP48	BUFG
6-Series	**1027**	**3382**	**1**	**0**	**1**
7-Series	**1077**	**3349**	**1**	**0**	**1**

Ordering information and related cores

Designation
MVD_ MPEGTS_AES_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses
Related cores : UDP/IP stack, RX RTP, TX RTP, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at *info_cores@mvd-fpga.com*