



Features

- Drop-in module for all xilinx FPGAs families
- 1 SPI input / 1 SPI output
- Compliant with DVB and ATSC standard
- Converts an MPEG TS constant mux rate into another (higher or lower)
- CPU configuration and monitoring interface
- Full PCR re-stamping
- External or internal output mux rate
- Input and payload bandwidth estimation
- Output smoothing FIFO
- Smoothing FIFO can be implemented as block RAM or external ZBT memory
- Configurable size of the smoothing FIFO
- Full synthesizable RTL design (not delivered) for easy customization
- Netlist version available for ISE 14.1 and later versions

Applications

Adaptive MPEG-TS bitrate may be used in applications related to transmodulation.

Description

The adaptive MPEG-TS core is a drop-in module for increasing or reducing the MPEG TS rate by filtering NULL packets.

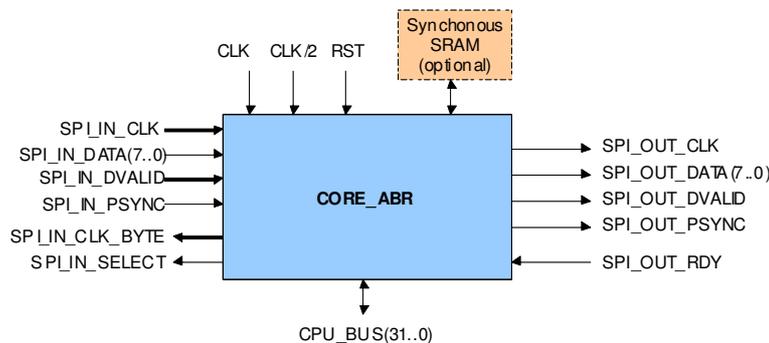
Input and output can be slave or master. In the last case, rate can be programmed.

The core provide counters such as :

- input bandwidth
- output bandwidth
- input payload
- smoothing FIFO usage

Large smoothing FIFO to optimize the bandwidth of the output rate.

Complete application fits into TBD depending on selected options.



Resource Utilization The core configuration may be set by conditional synthesis . Typical configuration with ZBT external memory.

	Slices	BRAMs	Mults/DSP48	Deliverables : Datasheet and Netlist for core generation
Spartan6	450	1*	1	

*depends on the use of the SRAM or not and the output FIFO depth requested

Ordering information and related cores

Parameters	Designation
BRAM	MVD_ADAPT_BRAM_NET
ZBT	MVD_ADAPT_ZBT_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : Cable Modulator J83B, DVB-C, DVB-S and/or DVB-T/H cores contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.