MPEG Closed caption Inserter Core V1.0

Product Brief (September 2013 - Rev A)

Description

The MPEG-TS closed caption inserter core is a drop-in module for insertion of DTV-708 closed caption into payload of MPEG video elementary stream.

The MPEG-TS closed caption inserter core can generate ATSC PSIP tables and is programmable thanks to a simple 8-bit CPU interface

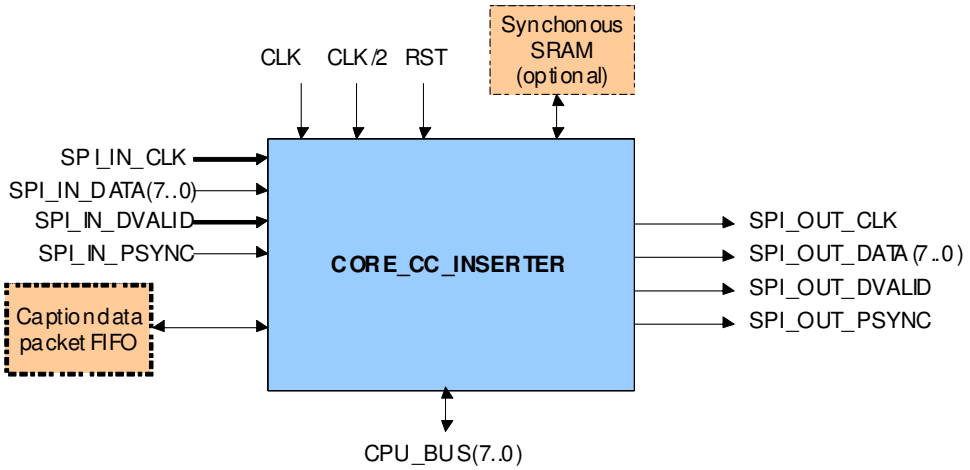
It includes full PCR re-stamping of the complete modified stream.

Applications

The MPEG-TS closed caption inserter core can be used in addition to an MPEG encoder module to add specifics functionalities and make it consistent in regards of PSIP ATSC standard.

Features

- **Drop-in module for 6 Series, 7 Series and later Xilinx FPGAs**
- **Interprets SMPTE-334 Caption data packet and insert the caption into the payload of the Video elementary stream.**
- **Can insert ATSC PSIP tables with dedicated Caption service descriptor and others "on demand" descriptors**
- **Rate of the stream is slightly increased to allow caption insertion and PSIP generation**
- **PCR restamping is done to make the output consistent**
- **8-bit CPU interface available for core control**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Resource Utilization

The core configuration may be set by conditional synthesis . Typical configuration without ZBT external memory.

	Slices	BRAMs 18k	DSP48
Spartan-6	**1700**	**6***	**1**

*depends on the use of the SRAM or not and the output FIFO depth requested

Ordering information and related cores

Parameters	***Designation***
BRAM	**MVD_CC_INSERTER_BRAM_NET**
ZBT	**MVD_CC_INSERTER_ZBT _NET**

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP Stack, UDP/RTP Transmitter, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator.

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.