MPEG USER DATA Inserter V1.0

Product Brief (July 2015 - Rev A)

Description

The MPEG-TS User Data inserter core is a drop-in module for insertion of user data into payload of MPEG video elementary stream.

The MPEG-TS User Data inserter core can manage up to 16 video payloads. The timing insertion is programmable thanks to 32-bit CPU interface.

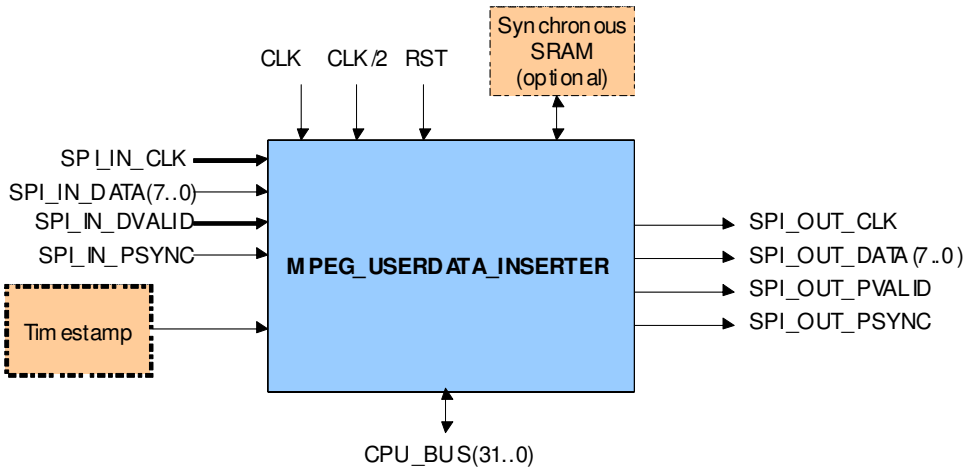
It includes full PCR re-stamping of the complete modified stream.

Applications

The MPEG-TS User Data inserter core can be used in addition to an MPEG recorder module to add specifics security information such as time and date of copy as well as original network identification.

Features

- **Drop-in module for 6 Series, 7 Series and later Xilinx FPGAs**
- **Insertion of user data into the payload of up to 16 Video MPEG elementary streams.**
- **Output rate of the stream is slightly increased to allow user data insertion.**
- **PCR restamping is done to make the output consistent.**
- **32-bit CPU interface available for core control**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Resource Utilization

The core configuration may be set by conditional synthesis . Typical configuration without ZBT external memory.

	Slices	BRAMs 18k	DSP48
Spartan-6	**741**	**3***	**1**
7 Series	**741**	**3***	**1**

*depends on the use of the SRAM or not and the output FIFO depth requested

Ordering information and related cores

Parameters	***Designation***
BRAM	**MVD_MUDI_BRAM_NET**
ZBT	**MVD_MUDI_ZBT _NET**

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP Stack, UDP/RTP Transmitter, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator.

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.