RTP Receiver V3.0

Product Brief (February 2013 - Rev A)

Features

- **Drop-in module for Spartan™-6, Virtex™-7, Artix™-7, Kintex™-7 and Zynq™ Xilinx FPGAs**
- **Full Hardware RTP Receiver**
- **Possibility to bypass RTP de-encapsulation to perform simple UDP de-encapsulation**
- **External Memory is mandatory for buffering incoming RTP packets to absorb network jitter, packets loss and packets disorder**
- **8MB Memory is required by RTP Receiver**
- **TS Payload only supported (for more Payload Type please contact MVD)**
- **Usable in routed network with an efficient de-jittering due to the field TIMESTAMP of RTP packets**
- **Clock compensation for 90kHz (Clock value for TIMESTAMP Transport Stream) ±100 ppm**
- **Efficient reordering packet (for packet loss and packet disorder)**
- **Netlist version available for ISE and VIVADO**

Description

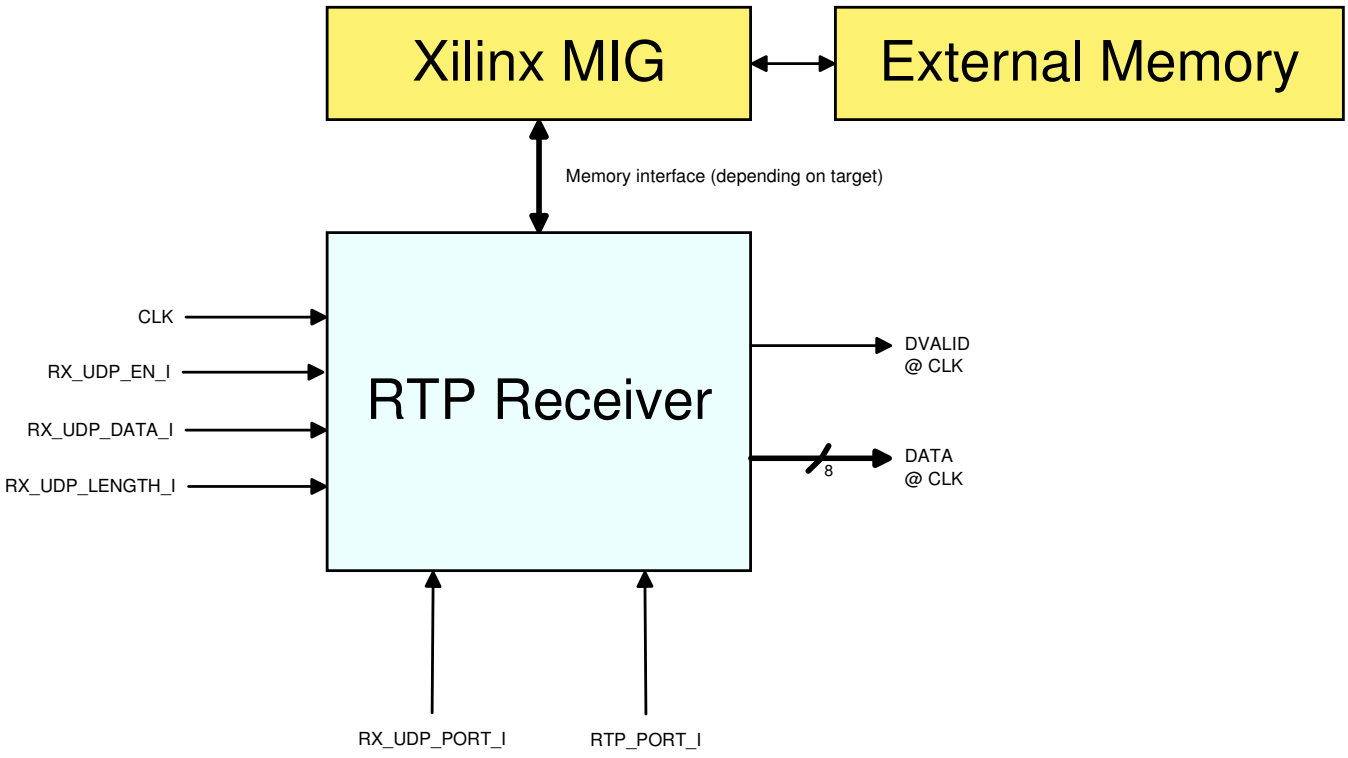
The MVD RTP Receiver allows the reception and the treatment of a RTP stream.

The RTP receiver stores the incoming RTP packets into external memory (for example in DDR3). During RTP packet reception, the RTP receiver analyses the different fields of the incoming RTP packet and reorder (if necessary) the incoming packet in the external memory. After the receiver has stored sufficient number of RTP packets(depending on RTP payload length), the RTP receiver will present on the output bus the valid data.

As the accepted payload is only MPEG2-TS, the used Timestamp clock value is only 90kHz. An efficient compensation for the clock value 90kHz is implemented inside the RTP Receiver which permits to compensate the clock drift (±100 ppm).

Applications

MVD RTP receiver can be used to receive UDP/RTP packets (or UDP packets only) on an Ethernet Network.
It may be used to receive IPTV UDP/RTP compliant stream in applications related to Multimedia transport.



Resource utilization

Without FEC option

	Slices	BRAMs (18k)	DSP48
Spartan-6 / 7 Series	550	2	1

With FEC option

	Slices	BRAMs (18k)	DSP48
Spartan-6 / 7 Series	800	4	1

Ordering information and related cores

Option	Designation
None	**MVD_RTP_RX_NET**
FEC	**MVD_RTP_ RX_FEC_NET**

VHDL source code: Can be delivered as an option under NDA and other specific clauses.
Related cores: MVD UDP/IP Stack, MVD RTP Transmitter, MVD Remultiplexer, MVD Modulators, ASI Transmitter.
Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.

Please contact us at *info_cores@mvd-fpga.com* for more information.