RTP Transmitter V3.0

Product Brief (April 2013 - Rev A)

Features

Full Hardware RTP transmitter

- **Drop-in module for Spartan™-6, Virtex™-7, Artix™-7, Kintex™-7 and Zynq™ Xilinx FPGAs**
- **Companion core of the MVD UDP/IP Stack IP core**
- **RTPv2 encapsulation**
- **Various Payload Type supported**
- **Support FEC Transmitter (optional)**
- **Variable RTP packet Payload length**
- **Computation of RTP Timestamp for RTP packets**
- **Possibility to bypass RTP Encapsulation to perform simple UDP Encapsulation for application which requires only UDP transmissions**
- **UDP compatible input**
- **Programmable Parameters of RTP and FEC (CPU interface)**
- **2D-FEC transmitter support (option) compliant with SMPTE 2022 only for MPEG-TS (Payload type 33)**
- **FEC option requires external memory**
- **Netlist version available for ISE and VIVADO**

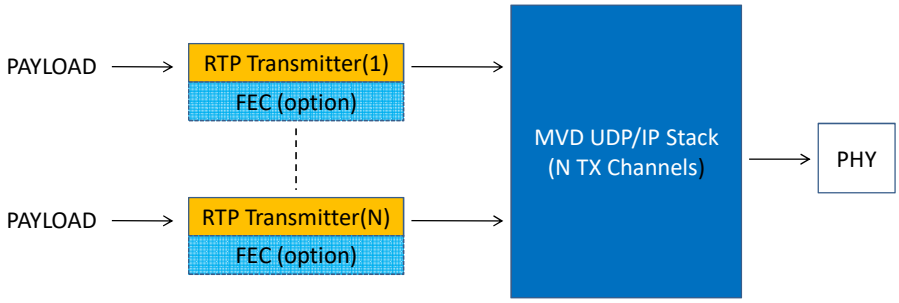
Description

This RTP Transmitter IP core implements a full Hardware RTP Transmitter.
If several channel are implemented into the FPGA, it allows sending RTP packets with a different payload type and different length on each channel.

Applications

MVD RTP transmitter is specially developed to transmit RTP flows on a routed network. It can be used to send IPTV compliant streams.

MVD UDP/IP Stack IP core is mandatory to use this core.



N parameter vary from FPGA ressources, Ethernet Speed connection and Number of Transmission channels requested.

Resource Utilization

Without FEC protection (Resources per RTP Transmitter)

	Slices	BRAMs (18k)	DSP48
Spartan-6	180	4	0
7-Series	160	4	0

With FEC protection (Resources per RTP Transmitter plus FEC option)

	Slices	BRAMs (18k)	DSP48
Spartan-6	520	4	0
7-Series	460	4	0

Ordering information and related cores

Option	Designation
None	**MVD_RTP_TX_NET**
FEC	**MVD_RTP_TX_FEC_NET**

VHDL source code: Can be delivered as an option under NDA and other specific clauses.

Related cores: MVD UDP/IP Stack, MVD Remultiplexers, MVD Modulators, ASI receiver …

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.

Please contact us at *info_cores@mvd-fpga.com* for more information.