RX MPEG-TS Interface V2.1
Product Brief (January 2015 - Rev A)

**Features**
- De-buffering and de-jittering MPEG-TS packets
- Drop-in module for Spartan-6™, Virtex-6™, Artix-7™, Kintex-7™ and Virtex-7™ FPGAs
- Single clock (125MHz or higher)
- Supports 188, 204 or 208 bytes packet input
- Supports Data Packet or Data Burst format
- Respects the PCR Accuracy according to TR 101 290 standard (+/- 500ns) (PCR mode)
- Auto-adaptation of frequency offset according to TR 101 290 standard (27MHz +/- 810Hz) (PCR mode)
- Programmable Latency
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist

**Applications**
RX MPEG-TS Interface may be used in applications related to IPTV and/or DVB/MPEG-2 transport streams.

**Description**
The MVD RX MPEG-TS Interface is a drop-in module that includes the following functions:
- 188, 204 or 208 bytes MPEG-TS input
- DVB-SPI interface output
- 188 bytes MPEG-TS output
- MPEG-TS packets output at regular intervals
- Bitrate calculation (with PCR) or bitrate estimation (without PCR)

**Resource Utilization**
The core configuration may be set by conditional synthesis.

<table>
<thead>
<tr>
<th>Series</th>
<th>Slices</th>
<th>LUTs</th>
<th>BRAMs (18k)</th>
<th>DSP48</th>
<th>BUFG</th>
<th>Deliverables</th>
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<td>Series-6</td>
<td>495</td>
<td>1830</td>
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<td>3</td>
<td>1</td>
<td>- Datasheet</td>
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<td>Series-7</td>
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<td>1</td>
<td>3</td>
<td>1</td>
<td>- Netlist for core generation</td>
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</tbody>
</table>

**Ordering information and related cores**

Designation
MVD_INTF_RX_MPEG_TS_NET

**VHDL source code**: can be delivered as an option under NDA and other specific clauses

**Related cores**: UDP/IP stack, RX RTP, TX RTP, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at info_cores@mvd-fpga.com