SAP/SDP Inserter Core V1.0

Product Brief (March 2018 - Rev A)

Features

- Drop-in module for Spartan™-6 and 7 Series Xilinx FPGAs
- Single clock
- Generates SAP Header and encapsulates SDP data into SAP packets
- SDP description (ASCII) is sent through CPU interface
- Can support up to 128 SAP/SDP Channels (if more channels are required please contact MVD)
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist (.ngc for Spartan-6 and .edn for 7 Series)

Description

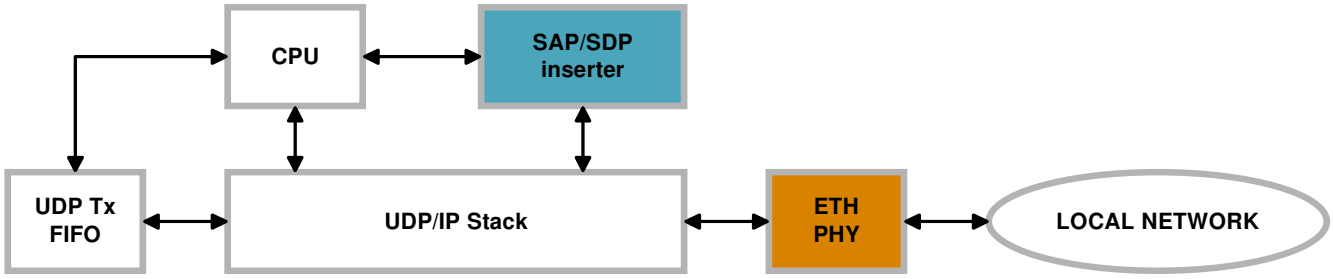
Session Announcement Protocol (SAP) is a protocol to broadcast multicast session information. SAP was published by the IETF as RFC2974.

The core encapsulates Session Description protocol (SDP) as a description of streaming media information. SDP was published by the IETF as RFC4566.

SAP/SDP inserter sends periodically SAP/SDP announcements at Multicast address 239.255.255.255 and UDP port 9875. These announcements allow the receivers which support SAP/SDP protocol to retrieve all the necessary information to connect to all streaming multicast media present.

Applications

The SAP/SDP Inserter Core is an add-on module for the MVD UDP/IP Stack that allows to send SAP/SDP packets for multicast stream announcements on a local network.



Resource Utilization

The following table describes resources utilization for 64 SAP/SDP Channels. Resources utilization depends on SAP/SDP channels required.

	Slices	BRAMs (18k)	DSP48
Spartan™-6	230	16	0
7 Series	220	16	0

Ordering information and related cores

Designation
MVD_SAP_SDP_Tx_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP stack, RTP Transmitter, Multi RTP Transmitter.

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