Serial Interface V3.0

Product Brief (March 2017 - Rev A)

Description

The Serial Interface is a companion core that can be used for MVD IP cores initialization.
It allows to set parameters and to read status.

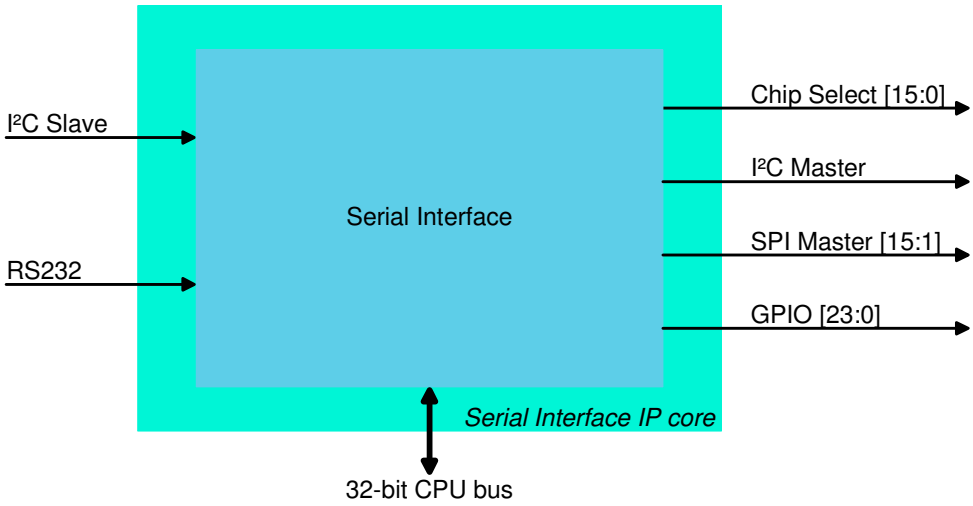
External input interface can be :

- **I2C 400KHz slave interface for 8-bit registers access**
- **UART interface with configurable Baud rates (from 9 600 to 921 600 Bauds), 8-bit, NO parity, 1 STOP bit**

The core can directly drive the 32-bit CPU interface of the MVD IP cores. It also delivers connection for master SPI, master I2C and GPIO interfaces.

Applications

The Serial Interface IP core can be used with any MVD IP core when local CPU is not available.



Resource Estimation

	Slices	BRAMs (18k)	DSP48	BUFG
Spartan-6	**280**	**1**	**0**	**1**
7 Series	**260**	**1**	**0**	**1**

Ordering information and related cores

Designation
MVD_MULTI_UDP_RTP_TS_RECEIVER_NET

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP stack, RTP Rx, RTP Tx, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at *info_cores@mvd-fpga.com*

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.

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