TS Jitter Cleaner core V2.0

Product Brief (July 2021 - Rev A)

Features

- **Drop-in module for Spartan™-6, 7 Series and later Xilinx® FPGAs**
- **Single clock**
- **Supports CBR input streams only**
- **Supports any packet length input from 188 to 255 bytes**
- **Supports data packet or data burst format**
- **External DDR memory mandatory for correct functioning in all cases**
- **Can manage up to 16 streams per instance (time multiplexed management)**
- **Number of stream managed are defined during netlist generation**
- **Reconstitute the flow rate of bursted or jitterized streams in which PCRs are corrects (+-500ns according to the standard)**
- **Auto-adjustment for a bitrate variation up to 32kbits without any discontinuity of the stream at the output**
- **For a bitrate variation higher than 32kbits and to ensure that the value is not corrupted, several bitrate calculation are performed before restarting the stream with the new bitrate**
- **Automatic selection for PID PCR or manually configurable in cases of some PCRs are wrong in the incoming stream**
- **Possibility to define a number of attempts for an incoming stream to lock on PCR value before entering in automatic bypass in case of wrong PCR at the input**
- **Bypass mode support in case of core should not be involved**
- **Bitrate accessible for each channel**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist .ngc or .edif formats**

Applications

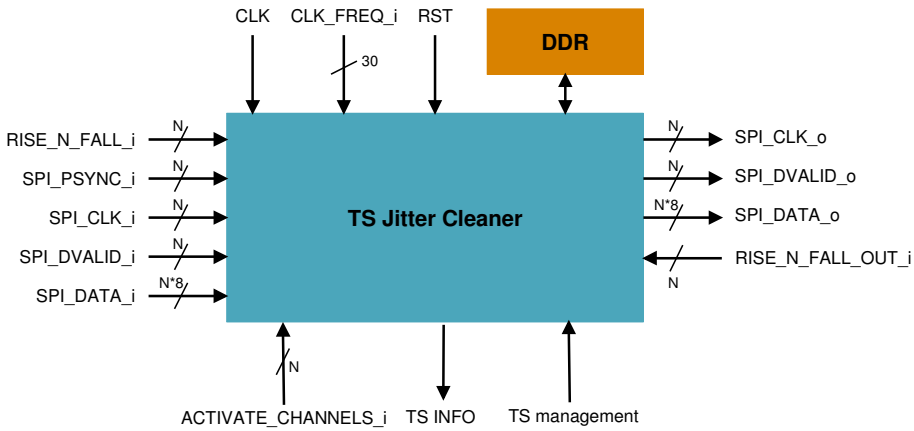
The TS Jitter Cleaner IP core is a module allowing to create DVB-SPI compliant stream from a CBR stream where MPEG-TS packets are not sent regularly (packets come in bursts) or suffer from jitter.

Description

All receiver equipments which have a DVB-SPI input must be fed with a stream which respects the timing between each PCR packet. The TS Jitter Cleaner IP core allows the transmission of an MPEG-TS data stream made of 188 bytes packets to such a receiver equipment with a DVB-SPI input.

The core is able to de-burst and de-jitter MPEG-TS packets of a CBR stream. The output respects PCR accuracy timing according to TR 101 290 standard.

The core can be configured to use BRAMs memory (if input streams have low jitter and/or bursts) or DDR memory (larger memory which permits to manage input streams with higher jitter and/or burst).



Resource Utilization (for 8 Channels)

Spartan-6 / 7-Series	Slices	BRAMs (18k)	DSP48
8 Channel	**2900**	**20**	**1**

Ordering information and related cores

Designation
MVD_TS_JITTER_CLEANER_NET

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP stack, RX RTP, TX RTP, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at *info_cores@mvd-fpga.com*