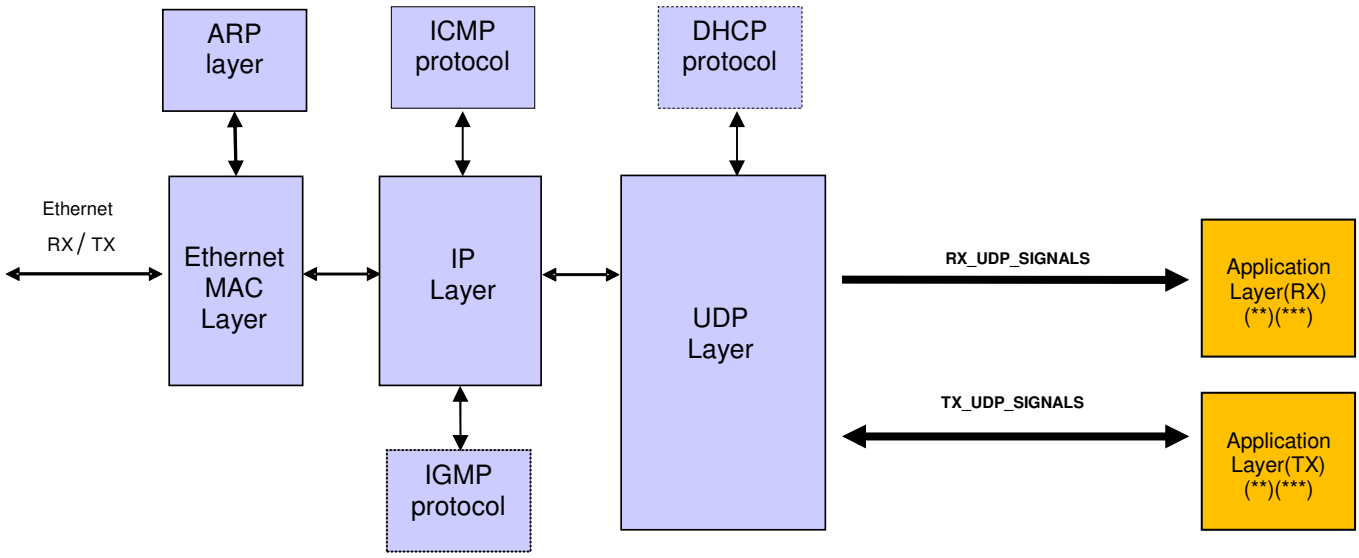
Full Hardware UDP/ IP stack V5.2

Product Brief (August 2017 – Rev A)

Description

The UDP/IP core is a drop-in module which includes its own MAC to send and receive UDP packets on an Ethernet Network.



(**) Applications layer not included in the core
(***) Application layer can be: FIFO, Modulators, top layer protocol over UDP such as RTP etc.

Applications

MVD Hardware UDP / IP stack may be used in applications related to Ethernet transmission with Xilinx Technology.

Resource Utilization

1x transmit UDP channel

	Slices	BRAMs (18k)	MULT or DSP48
Spartan™-6	**2 500**	**7**	**0**
7-Series	**2 450**	**7**	**0**

32x transmit UDP channels

	Slices	BRAMs (18k)	MULT or DSP48
Spartan-6	**3100**	**16**	**0**
7-Series	**3100**	**16**	**0**

- Raw Frame and Jumbo Frames support are not taken in account for the resources estimation
- Resources can be spared if some protocols are not needed.

Features

- **Drop-in module for Spartan™-6, Virtex™-7, Artix™-7, Kintex™-7 and Zynq™ Xilinx FPGAs**
- **GMII default interface (GMII-to-RGMII option / SGMII with Xilinx Logicore IP *Ethernet 1000BASE-X PCS/PMA or SGMII)***
- **MAC Layer is included in the core (support of Ethernet Frame II)**
- **Compatible with 10/100/1000 Ethernet mode**
- **Supported protocols :**
    - **IPv4**
    - **UDP**
    - **ARP (for Request and Reply)**
    - **ICMP**
    - **IGMPv3 (supports IGMPv2 for backward compatibility)**
    - **DHCP client**
    - **VLAN Rx / Tx (supports IEEE 802.1 Q Frame)**
- **IPv4 fragmentation not supported**
- **Support up to 8 Multicast Address for Reception (can be increased if needed but will require more FPGA resources)**
- **Netlists delivered for 1, 2, 4, 8, 16, 24 and 32 transmit UDP channels**
- **Management of ARP table up to UDP output channels count (if UDP output channels count ≥ 2)**
- **Point to Point UDP Transmission Channel for well known Link**
- **Jumbo frames up to 9kB (requires FPGA internal memory, delivered on demand)**
- **Raw Frames (requires FPGA internal memory, delivered on demand)**
- **Differential Services (QoS) programmable for each UDP transmit channel**
- **TTL IP Layer programmable for each UDP transmit channel**
- **Support up to 8 different VLAN ID tag for Ethernet Reception (can be increased if needed)**
- **Support up to 8 different VLAN ID tag for for each UDP transmit channel (can be increased if needed)**
- **Netlist version available for ISE and VIVADO**

Ordering information and related cores

Designation
MVD_UDP_IP_NET

VHDL source code: Can be delivered as an option under NDA and other specific clauses.

Companion cores: Serial Interface for CPU configuration.
Related cores: ASI receiver, MVD modulators…

Documentation and support: Datasheet and user's guide. In addition MVD can provide on site or remote coaching.

Please contact us at *info_cores@mvd-fpga.com* for more information.