UPCONVERTER for AD9739/A V2.1

Product Brief (May 2017 - Rev B)

Features

Converts multiple baseband I-Q signals to analog RF signal with AD9739 or AD9739A 14-bit RF DAC sampled at up to 2.5 GHz

- **Drop-in module for Spartan-6™, Virtex-6™, Artix-7™, Kintex-7™ and Virtex-7™ FPGAs**
- **Provides direct RF synthesis for baseband I-Q signals (DC to 1.25 GHz)**
- **Support for 2nd and 3rd Nyquist zone for carriers frequencies up to 3GHz+**
- **Includes clock management module**
- **Very low FPGA resources required**
- **32 or 64 MHz minimum bandwidth per RF channel**
- **In-band ripple < 0.2 dB and SNR > 75dB**
- **Carrier frequency dynamically adjustable with sub-Hertz precision**
- **Dual 14-bit LVDS output busses directly tied to AD9739/A input data pins (compatible with 11-bit for AD9737A)**
- **Can be modified for using others RF DAC (please contact MVD)**
- **Fully synthetizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlists + VHDL design example**

Applications

The Upconverter for AD9739/A is recommended for digital TV transmission and other telecommunication systems requiring low noise and adjustment free RF stages.

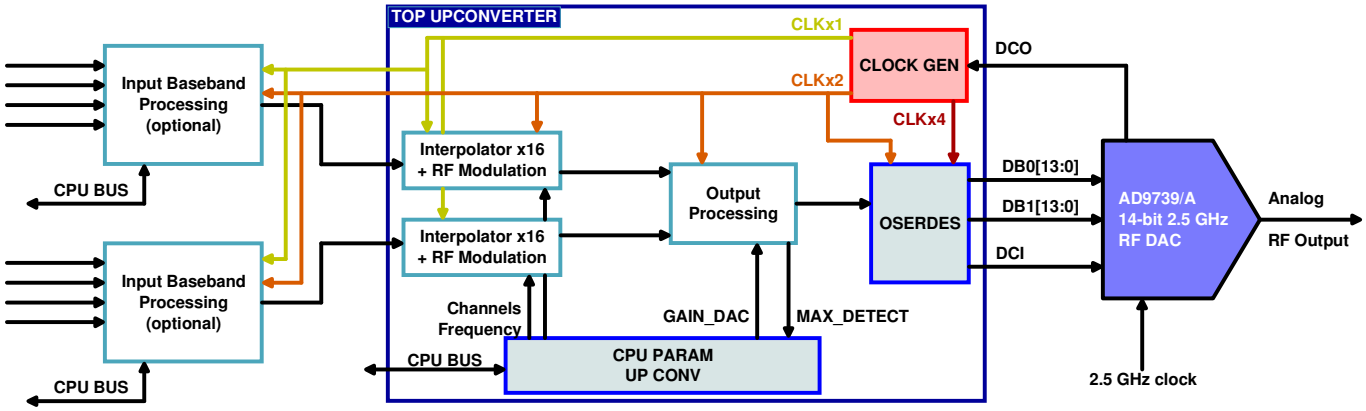
Description

The MVD Upconverter core is a drop-in module that includes the following functions :

- **An Interpolation x16 + RF Modulation per each independent RF channel**
- **An Output Processing module which combines up to 32 independent RF interpolator channels**
- **A clock management module**
- **An OSERDES module which connects the LVDS IO to the RF DAC**
- **A CPU BUS to configure the parameters of the Upconverter**

Companion cores

- **Input Baseband Processing core for Upconverter**
- **SPI Configuration core for AD9739/A**



The available bandwidth varies with the sampling frequency chosen for the DAC:

Fdac	2100 MHz	2300 MHz	2500 MHz
Standard Version	32 MHz	35 MHz	38.1 MHz
Wide Version	64 MHz	70 MHz	76.2 MHz

Resource Utilization

NOTA : The following resources don't take account of the Input Baseband Processing core's resources. If the Input Baseband Processing core is used before the Upconverter, please add, the resources of this core (according the number of input baseband signals per Input Baseband Processing module) multiplied by the number of the Upconverter's independent RF channels, to the following resources.

For 1 channel :

	Slices (LUT)		BRAMs (18k)	DSP48	BUFG	PLL
	Standard	Wide				
Spartan-6 TM	**1900** (7600)	**2200** (8800)	**8**	**24**	**3**	**1**
V6 or Series-7 TM	**1700** (6800)	**2000 (**8000)	**8**	**24**	**3**	**1**

For 2 channels :

	Slices (LUT)		BRAMs (18k)	DSP48	BUFG	PLL
	Standard	Wide				
Spartan-6 TM	**3550** (14200)	**4200** (16800)	**16**	**40**	**3**	**1**
V6 or Series-7 TM	**3200** (12800)	**3800** (15200)	**16**	**40**	**3**	**1**

For 4 channels :

	Slices (LUT)		BRAMs (18k)	DSP48	BUFG	PLL
	Standard	Wide				
Spartan-6 TM	**6850** (27400)	**8150** (32600)	**32**	**80**	**3**	**1**
V6 or Series-7 TM	**6200** (24800)	**7400** (29600)	**32**	**80**	**3**	**1**

Ordering information and related cores

Version	***Designation***
Standard – 32/38 MHz bandwidth	**MVD_UPCONV_STD_N_RF_2.5GBS_NET**
Wide – 64/76 MHz bandwidth	**MVD_UPCONV_WIDE_N_RF_2.5GBS_NET**

NOTA : N = Number of RF channels (1, 2, 4, 8, 16 or 32)

VHDL source code : can be delivered as an option under NDA and other specific clauses

Complementary cores : Input Baseband Processing core, SPI Configuration core for AD9739/A.

Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator, ATSC Remultiplexer, ASI Receiver, ASI Transmitter, Input Baseband Processing, Interpolator x16 + RF Modulator or Output Processing cores contact us at *info_cores@mvd-fpga.com*

Documentation and support : Datasheet. In addition MVD can provide on site or remote coaching.