

Features

Converts complex baseband I-Q signal @ F_{symbol} rate to complex baseband or IF I-Q signal @ F_{clock} DAC.

Compliant with all our cable and terrestrial modulators (DVB-C J83A/C, J83B, ATSC, DVB-T/T2)

- Drop-in module for Spartan-6™, Virtex-6™, Artix-7™, Kintex-7™, Virtex-7™ FPGAs and Zynq™
- Dual clock (1x,2x), CLK 1x frequency equal to DAC clock frequency (up to 160 MHz)
- Includes Symbol rate generator
- Programmable RRC filter for cable modulators (J83B : 0.12 or 0.18, DVB-C/J83A : 0.15, ISDB-C/J83C : 0.13)
- Programmable symbol rates for cable modulators (from 5MSymb/s to 7MSymb/s)
- Programmable output bandwidth for DVB-T/T2 (1.7, 5, 6, 7, 8 or 10 MHz)
- Programmable output bandwidth for ISDB-T (6, 7 or 8 MHz)
- Can act as Master or Slave for symbol rate generation
- Complex baseband or IF outputs (2 x 16 bits) @ F_{clock} DAC
- Possible selection on the fly modulation (optional)
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- SNR > 60dB

Applications

The UPSAMPLER is recommended for using DAC which has no upsampling stage. The application is for digital TV transmission system requiring low noise and filter adjustment stages.

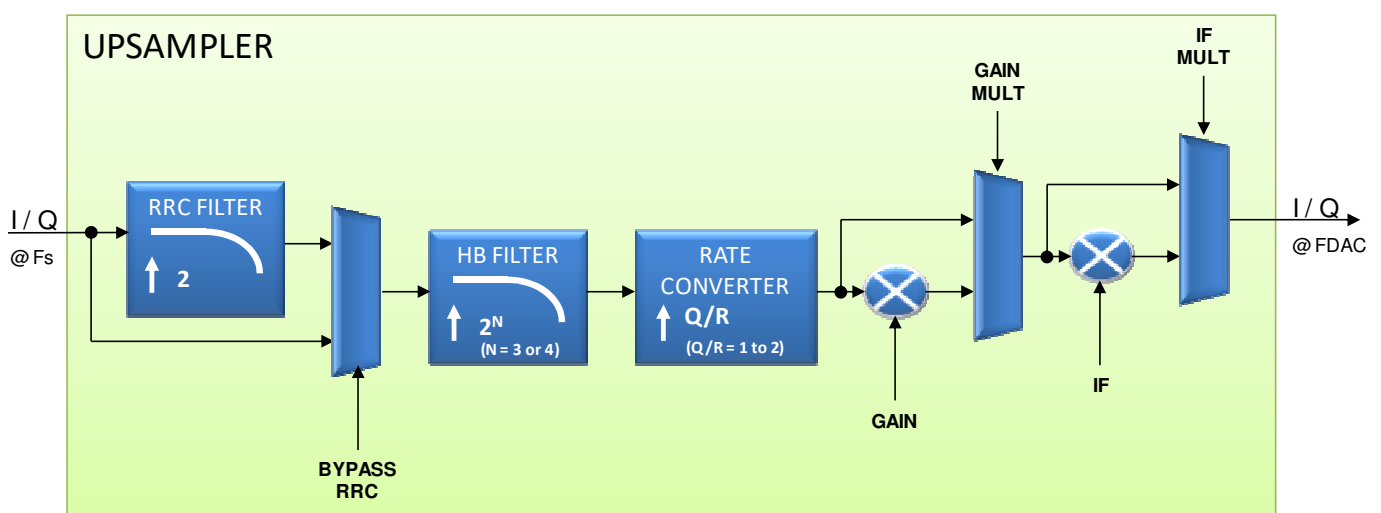
Description

The UPSAMPLER core is a drop-in module that includes the following functions :

- RRC filter for J83 cable application
- Half-Band filters to interpolate the signal
- Rate Converter to adjust the signal's rate from 1.0 to 2.0
- Optional gain multiplier
- Optional Intermediate Frequency multiplier
- Output for complex DAC (2 x 16 bits)

Companion cores

- DVB-C/J83AC modulator core
- J83B modulator core
- ATSC modulator core
- DVB-T modulator core
- DVB-T2 modulator core
- ISDB-T modulator core
- Serial Interface for CPU configuration



Resource Utilization

The user can dynamically modify the UPSAMPLER core configuration to select the modulation to be used. If no on the fly modulation selection is required, the input signal MOD_CONF_i can be tied to the desired modulation value. For fixed modulation the resources are listed above:

J83A/C, DVB-C, J83B application resources :

```
constant MOD_CONF : std_logic_vector(1 downto 0) := "00";
```

	Slices	LUT	BRAMs (18k)	DSP48	BUFG
Series-6™	580	2120	0	10	3
Series-7™	580	2120	0	10	3

ATSC application resources :

```
constant MOD_CONF : std_logic_vector(1 downto 0) := "01";
```

	Slices	LUT	BRAMs (18k)	DSP48	BUFG
Series-6™	500	1850	0	6	3
Series-7™	500	1850	0	6	3

DVB-T/T2 application resources :

```
constant MOD_CONF : std_logic_vector(1 downto 0) := "10";
```

	Slices	LUT	BRAMs (18k)	DSP48	BUFG
Series-6™	560	2080	0	8	3
Series-7™	560	2080	0	8	3

ISDB-T application resources :

```
constant MOD_CONF : std_logic_vector(1 downto 0) := "11";
```

	Slices	LUT	BRAMs (18k)	DSP48	BUFG
Series-6™	550	2050	0	8	3
Series-7™	550	2050	0	8	3

GAIN multiplier resources :

```
constant GAIN_MULT : std_logic := '1';
```

```
-- '0' : DELETE GAIN MULTIPLIER, '1' : ADD GAIN MULTIPLIER
```

	Slices	LUT	BRAMs (18k)	DSP48	BUFG
Series-6™	+ 15	+ 50	0	+ 1	0
Series-7™	+ 15	+ 50	0	+ 1	0

IF multiplier resources :

```
constant IF_MULT : std_logic := '1';
```

```
-- '0' : DELETE IF MULTIPLIER, '1' : ADD IF MULTIPLIER
```

	Slices	LUT	BRAMs (18k)	DSP48	BUFG
Series-6™	+ 60	+ 230	+ 1	+ 4	0
Series-7™	+ 60	+ 230	+ 1	+ 4	0

Ordering information and related cores

Parameters	Designation
CPU programmable	MVD_UPSAMPLER_CPU_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses.

Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB-T2, ISDB-T, DVB Remultiplexer and/or ASI interface cores, contact us.

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.