Multi Channel Up Converter for direct RF synthesis using MAX5881 Maxim RF DAC@4.2Gs/sec

Product Overview (November 2009 - Rev A)

Features

Converts multiple base band I/Q channels to RF in the range 50MHz to 2GHz.
Can be customized for a wide range of applications for any number of channel types and bandwidth

Applications

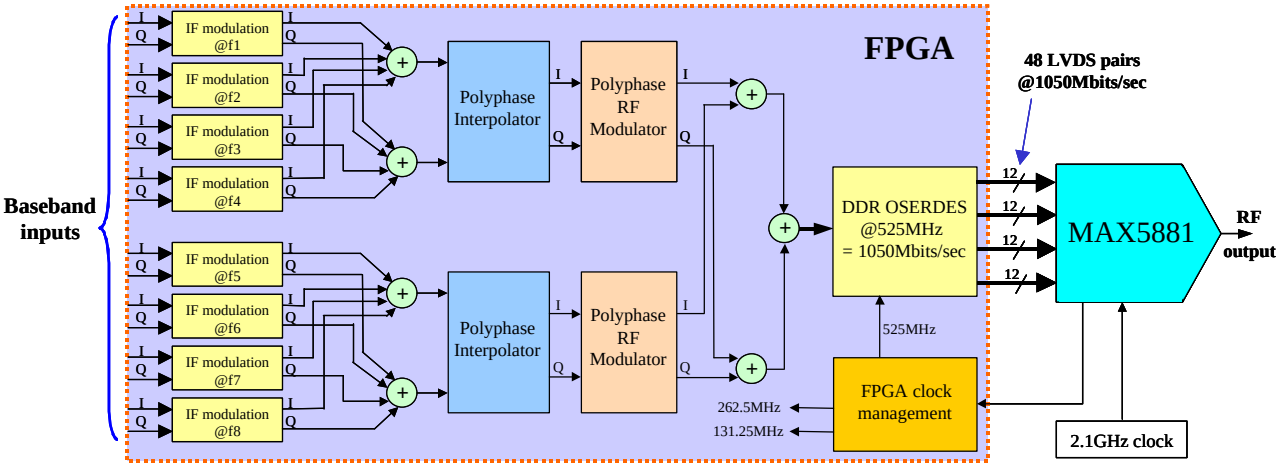
Broadband Communication Systems
Cellular infrastructure
Edge QAM devices
Cable Modem Termination Systems (CMTS)
Video-On-Demand (VOD)

FPGA targets

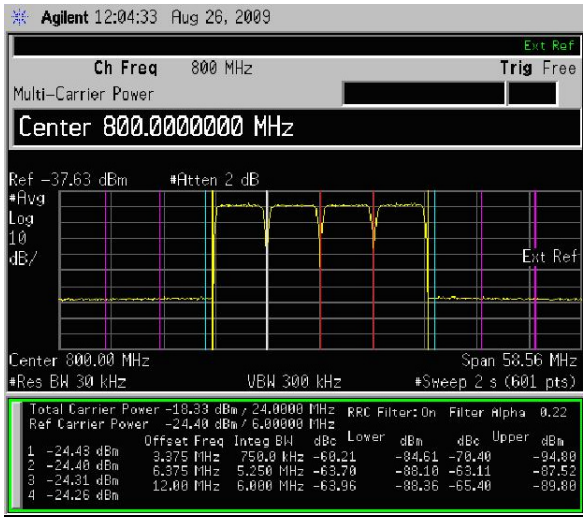
- **Spartan-6**
- **Virtex-5**
- **Virtex-6**

Companion cores

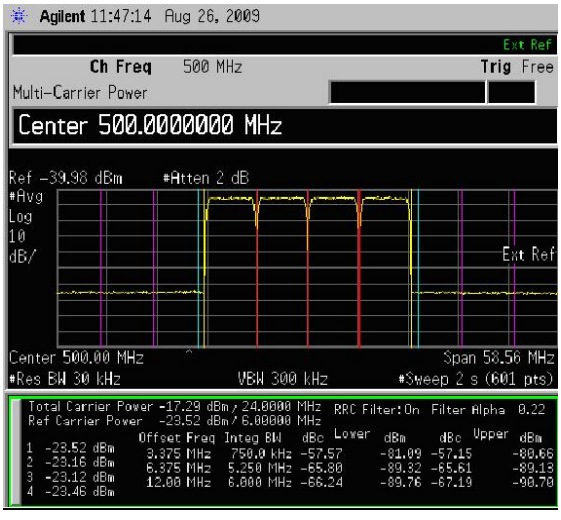
- **ASI receiver**
- **DVB remultiplexer**
- **DVB-C modulator**
- **CMTS modulator**
- **DVB-T/H modulator**
- **ATSC / 8VSB modulator**



Block diagram example for 2 groups of 4 CMTS/DVB-C or DVB-T channels



Group of 4 QAM64 channels @800MHz



Group of 4 QAM256 channels @500MHz

Performance measurement examples
(demo available on MAXIM HSDCEP board)

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RF frequency range For Fdac = 4.2 Gs/sec	*In band spurious noise @Fdac/2 - Fout*	*Noise floor*	*ACP1*	*ACP2*	*ACP3*
50MHz to 1GHz	*Out of band*	*-58dB*	*-60dB*	*-62dB*	*-63dB*
1GHz to 2GHz	*-43dB*	*-56dB*	*-56dB*	*-57dB*	*-58dB*
Performance numbers for 2 groups of 4 J83B QAM channels					

MVD takes advantage of the advanced FPGA features and development techniques for very high performance DSP functions implementation. The Spartan-6, Virtex-5 and Virtex-6 architectures provide advanced features necessary for this very high speed (4GHz+) advanced Up Converter.

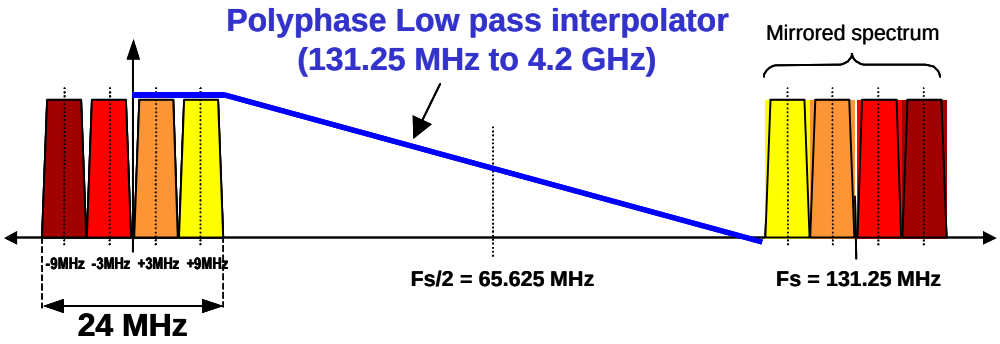
Among those important features :

- Powerful and flexible slice logic
- Very fast distributed memory & block RAM
- Embedded cascadable DSP bocks
- High speed clocks managements
- IO SERDES & LVDS IOs for 1GHz+ data rate while working at lower speed in the FPGA fabric

Required resources depend on the number of channel groups and channels per group to be modulated. As an example, the input streams can be base band I & Q signals sampled at 131.25 MHz.
Each channel is then modulated at a low Intermediate Frequency as follows : for 6MHz wide channels grouped by 4, the respective IF frequencies can be –9MHz, -3MHz, +3MHz and +9MHz. This group behaves as a 24MHz wide base band channel (Intermediate Frequency = 0MHz).

To reach 1050 Mbits/sec on the 4 x 12 links from the FPGA to the MAX5881 RF DAC (working @4.2 Gsps), the Spartan-6, Virtex-5 or Virtex-6 IO SERDES allow to distribute the several output phases of the modulator with precharacterized performance (independently of Place & Route optimization) : In those families, all IOs have an embedded ISERDES and OSERDES, able to work in SDR or DDR mode. They support 1050 Mbits/s rate, while serializing internal data (4 to 1 or 8 to 1 in our case), originally sampled at much lower frequency (131.25 MHz for Spartan-6 or 262.5 MHz for Virtex-5 and Virtex-6).

Demonstration bitstream is available on Maxim HSDCEP (Virtex-5LX110) + MAX5881 eval boards.



VHDL source code : can be delivered as an option under NDA and other specific clauses
Related cores : Cable Modulator J83B, DVB-S, DVB-C, DVB-T, ATSC-8VSB, DVB Remultiplexer and ASI Receiver cores
For additional information, please contact us at ***info_cores@mvd-fpga.com***
Documentation and support : The Up Converter core is delivered as a customized application, upon customer requirements. In addition MVD can provide on site or remote coaching.

MVD Cores	**106 Avenue des Guis** **31830 Plaisance du Touch** **France**