MVD Cores solutions for Multi channel Direct RF synthesis using RF DACs with low cost or high performance FPGAs

During the last few years, the DAC technology evolved so much that it's easy now to build the RF part of a modulator using exclusively digital technologies.

Fortunately, the FPGA architectures and performance also evolved so much, so it's the ideal way to drive those very high performance DACs. Among the main FPGA improvements necessary for this kind of applications :

- Digital Signal Processing blocks and related logic
- Powerful slice logic for complementary processing
- I/O SERDES for high speed data transfer required to drive such DACs (1Gbit/sec to 1.25 Gbit/sec x number of data lines)
- PLL technology capable of synthesizing 1GHz+ internal clocks with very low jitter

Those features are available on the mature Virtex-5 architecture, easily transposable to the latest Virtex-6 family, but are also available in the low cost **Spartan-6** family.

Spartan-6 is a low cost FPGA family that includes features (PLL, I/O SERDES, DSP blocks, new CLB and slice architecture) only available on high end FPGA families on the previous families.

Today available DACs for direct RF synthesis are :

- AD9739: 14-bit, up to 2.5 Gs/s from Analog Devices. For example, requires 2 x 14-bit LVDS data lines @1.050 Gbit/s for 2.1 GHz sampling frequency. (28 LVDS inputs)

- DAC5670: 14-bit, up to 2.4 Gs/s from Texas Instruments

- MAX5881: 12-bit, up to 4.3 Gs/s from Maxim. Requires 4 x 12-bit LVDS data lines @ 1.050 Gbit/s for 4.2 GHz sampling frequency (48 LVDS inputs)

- MAX5879: 14-bit, up to 2.3 Gs/s from Maxim. Requires 2 x 14-bit LVDS data lines @ 1.050 Gbit/s for 2.1 GHz sampling frequency (30 LVDS inputs)

All these RF DACs can be driven by the low cost Spartan-6 or high end Virtex-6 or Virtex-6 FPGA family.

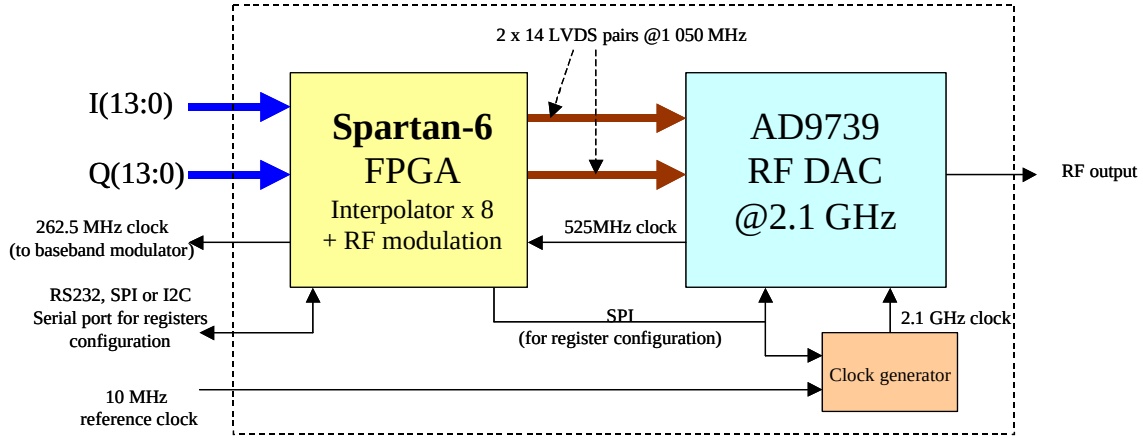
As an example, for applications, a 16-channel 2.1 Gs/sec up converter EURODOCSIS compliant (128 MHz available bandwidth) can be implemented into a very small and cheap 6SLX16 !!!

Of course, in most applications, the user may require to implement many DVB-x modulators in the same FPG A, so more logic resources will be required..
MVD Cores offers a wide range of solutions for Up Converter implementation on FPGA.

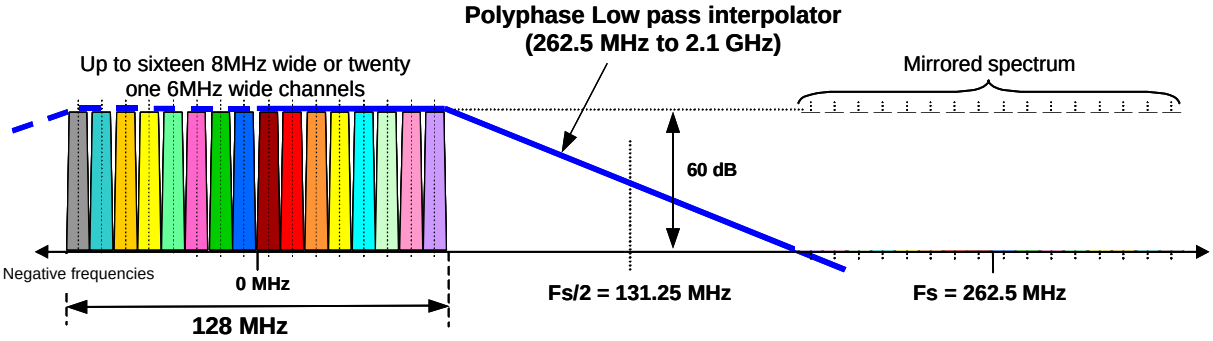
- Reference designs for demonstration/evaluation (see next pages for MAX5881 + HSDCEP reference design, based on Virtex-5)
- Custom design (netlist or source code) upon your own specifications (Spartan-6, Virtex-5, Virtex-6)
- Source code of a reference design + know how transfer & training for customization by the users
- In addition, MVD provides training on Xilinx technologies (training provider ATP) and on site or remote consulting services. Among the available training, "DSP Implementation Techniques" a 2-day training to understand how to efficiently use the amazing feature of the Xilinx FPGA architectures.

Application examples :

- **Low cost high performance Up Converter with AD9739 + Spartan-6**



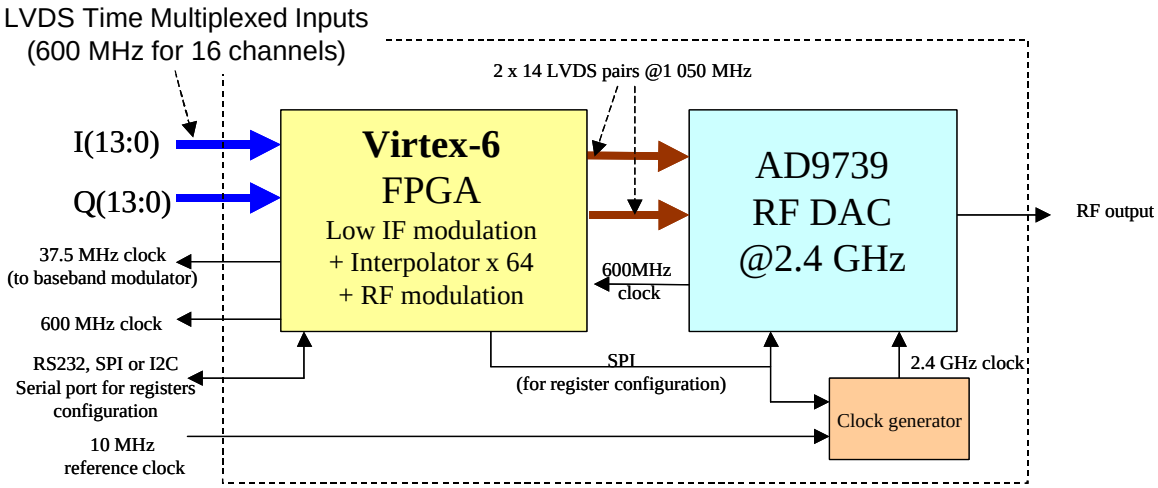
This figure shows the DOCSIS compliant Up Converter + DAC part of a modulator with direct RF synthesis that covers the band of 50MHz to 1000MHz. The DAC is sampled @ 2.1 GHz. The baseband I and R signals feed the x64 interpolator implemented into the low cost Spartan-6 FPGA. The interpolator bandwidth allows to fit up to sixteen DVB-C or DVB-T channels each one being 8 MHz wide, or twenty one 6MHz wide channels. The input channels must be first modulated at low Intermediate Frequency as follows :



By taking advantage of the Spartan-6 unprecedented features on low cost FPGA architectures, this design fits into one of the smaller available part : XC6SLX16. For multi-channel application, this example however requires that the several I and Q channels are modulated at a low Intermediate Frequency, as shown in the figure. MVD Cores can provide technical assistance and/or complementary DSP functions for this.

- **Very high channel count DOCSIS and EURODOCSIS designs : Virtex-6 + AD9739**

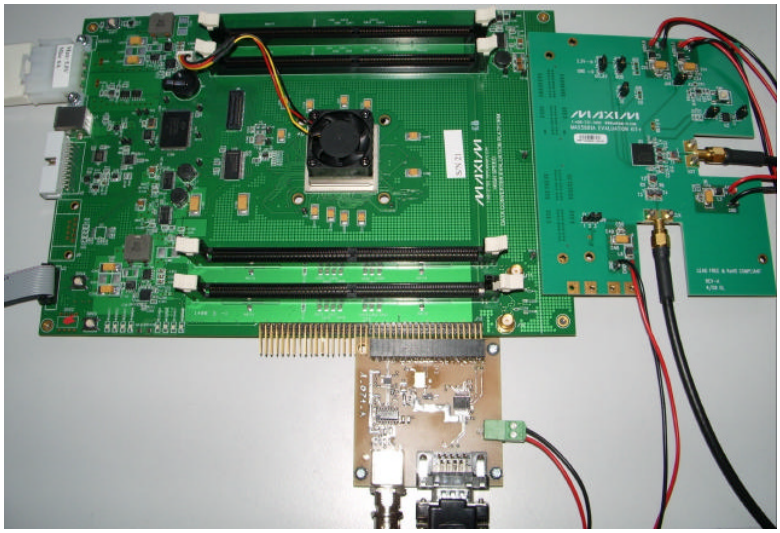
For higher channel count, MVD recommends using the Virtex-5 or Virtex-6, high density/high performance FPGA family with the AD9739 RF DAC. In this case, the DAC can work at 2.4 to 2.5 Gs/s to cover the band 0 MHz to 1200 MHz.



Much more and higher speed DSP functions can be implemented on the Virtex families. For example, with a single FPGA, a complete application for 32 to 64 DVB (or J83B) channels can be implemented from ASI or SPI input to RF output can be implemented.

- **Using Virtex-5 or Virtex-6 + Max5881 sampled @4.2 GHz :**

A similar strategy can be used with the MAX5881 RF DAC with a sampling rate of up to 4.3 Gs/s.
You can see on the next pages the description of a reference design for an 8-channel Up Converter implemented on the Maxim HSDCEP board with the MAX5881 eval board.
The HSDCEP board was developed by Maxim for the MAX5881 RF DAC users. It's equipped with a Virtex-5 Xilinx FPGA (XC5VLX110).



For more information about the MVD reference design on HSDCEP board, have a look, on the following link :
http://www.mvd-fpga.com/cores/en/files/MVD_Up_Converter_for_MAX5881_Core_Overview.pdf