

Features

Multi mode ASI receiver

- European standard EN50083-9 Annex B
- Drop-in module for Virtex-6™, Virtex-5™, Virtex-4™, Spartan-6™ and Spartan™-3/E/A FPGAs
- 135MHz Single Clock (27MHz supported for Spartan-6™ and Virtex-6™)
- Supports 188 or 204 bytes packet input
- Supports direct ASI interface (clock recovery from Data)
- Supports Data Packet or Data Burst format
- Single channel – support for multi channel
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist

Applications

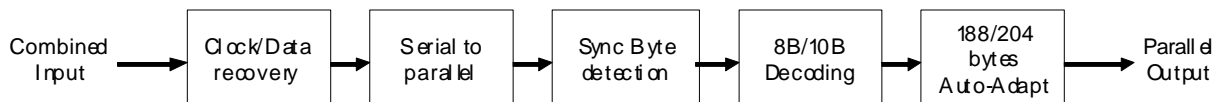
ASI Receiver may be used in applications related to DVB/MPEG-2 transport streams.

Description

The MVD ASI receiver core is a drop-in module that includes the following functions :

- Clock/Data recovery
- Serial/parallel Conversion
- Sync Byte (FC Comma Detection)
- 8B/10B decoding
- Auto adaptation to 188/204 bytes packet Input
- 188 bytes MPEG-TS output

No external components required (1)



ASI receiver core requires a 270 MHz reference clock usually internally generated with a 135MHz external oscillator. Consult us for more details on clock generation and distribution.

Resource Utilization The core configuration may be set by conditional synthesis .

		Slices	Clock Buffer	Clock Component		
1 Channel	Spartan3/E/A	180	6 BUFG	4 DCM	Deliverables : Datasheet Netlist for core generation	
	Spartan-6, Virtex 5/6	80	6 BUFG	1 PLL		
4 Channels	Spartan3/E/A	730	6 BUFG	4 DCM		
	Spartan-6, Virtex 5/6	300	6 BUFG	1 PLL		
<i>(values may vary depending on implementation options)</i>						

Ordering information and related cores

Designation
MVD_ASI_RX_NET

(1) External equalizer and/or transformer is recommended for long cable interfaces.

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Transmitter cores, contact us at info_cores@mvd-fpga.com