

Features

ATSC A/53 Part 2

- The MVD ATSC modulator core is delivered for baseband output to be natively connected to AD9789 DAC from Analog Devices but can be used in Intermediate Frequency application (for Analog Devices (AD9744)) or in RF application when respectively connected to our UPSAMPLER or our UPCONVERTER core (for Analog Devices (AD9739A) or Maxim RF DACs (MAX5881)).
- Drop-in module for Spartan-6™, Virtex-6™, Artix-7™, Kintex-7™, Virtex-7™ FPGAs and Zynq™
- Single clock (up to 160 MHz)
- Robust SPI input (discarding incorrect input packets)
- PCR re-stamping
- Complex baseband outputs (2 x 16 bits) @ Fsymbol rate
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist

Applications

The ATSC modulator may be used in applications related to terrestrial transmission, typically at the cable head end.

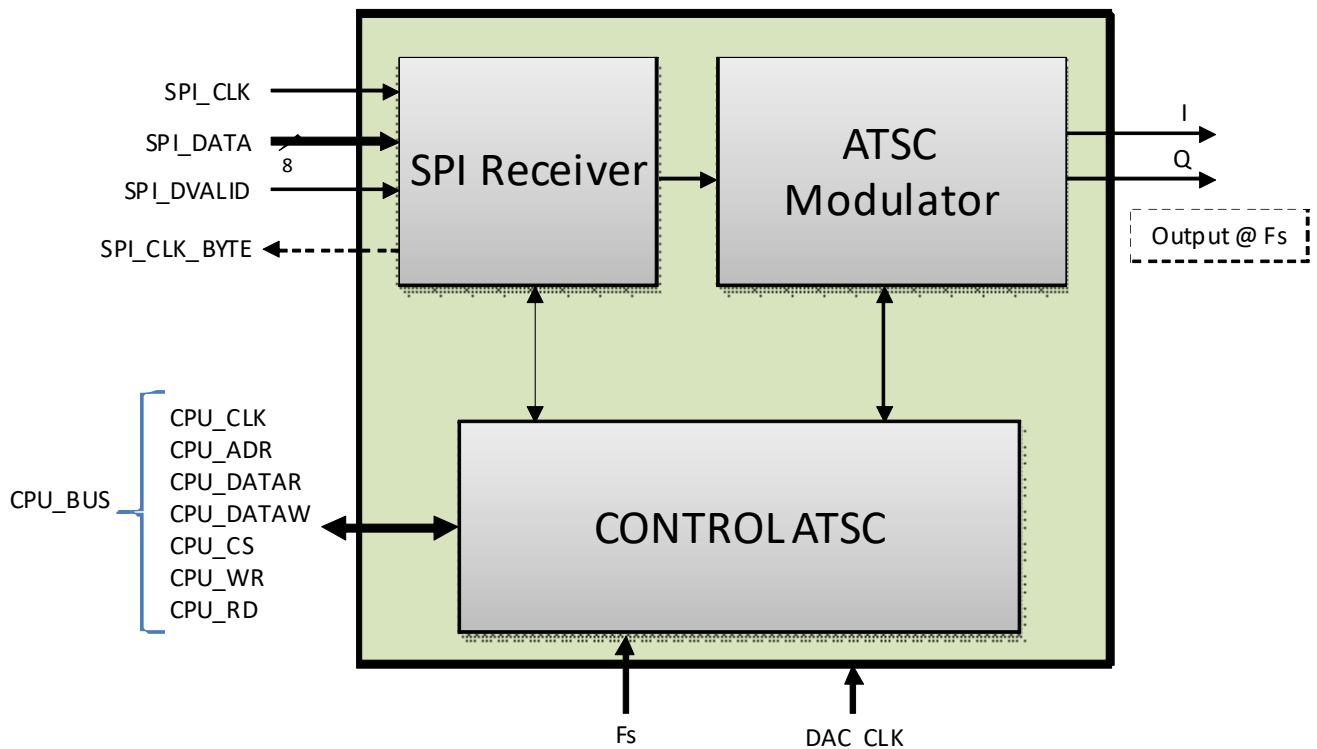
Description

The MVD ATSC core is a drop-in module that includes the following functions :

- Input data framer from DVB-SPI source (MPEG-TS flow)
- ATSC modulator (Energy dispersal, Reed-Solomon encoder, interleaver, trellis encoder)
- VSB modulator
- Output for complex DAC (2x16bits)

Companion cores

- ASI receiver core
- ATSC Remultiplexer
- Serial Interface for CPU configuration
- I2C slave Interface core



Resource Estimation

	Slices	LUTs	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables :
Series-6	1100	3410	6	12	2	- Datasheet
Series-7	1100	3410	6	12	2	- Netlist for core generation

Ordering information and related cores

Parameters	Designation
CPU programmable	MVD_ATSC_AD9789_CPU_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer and/or ASI Receiver cores
contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.