



Features

ITU-T J.83 Annex B
 Compliant baseband transmitter for Cable Modem Termination Systems (CMTS)

- The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)
- Drop-in module for Virtex-6™, Virtex-5™, Virtex-4™, Spartan-6™ and Spartan™-3/E/A FPGAs
- Single clock (up to 140 MHz+ for Spartan-3/6™, 180 MHz+ for Virtex-4/5/6™)
- Robust SPI input (discarding incorrect input packets)
- PCR re-stamping
- Supports 5.056941 & 5.360537 symbol rates
- Programmable 64 and 256 QAM Symbol Mapping
- All interleaver modes supported thanks to external Synchronous SRAM
- Intermediate frequency output for single DAC (14 bits) or baseband outputs (2 x 16 bits)
- Single channel – support for multi channel
- Fully synthetizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 42dB

Applications

Cable modulator J83B – 4 channel may be used in applications related to cable transmission, typically at the cable head end.

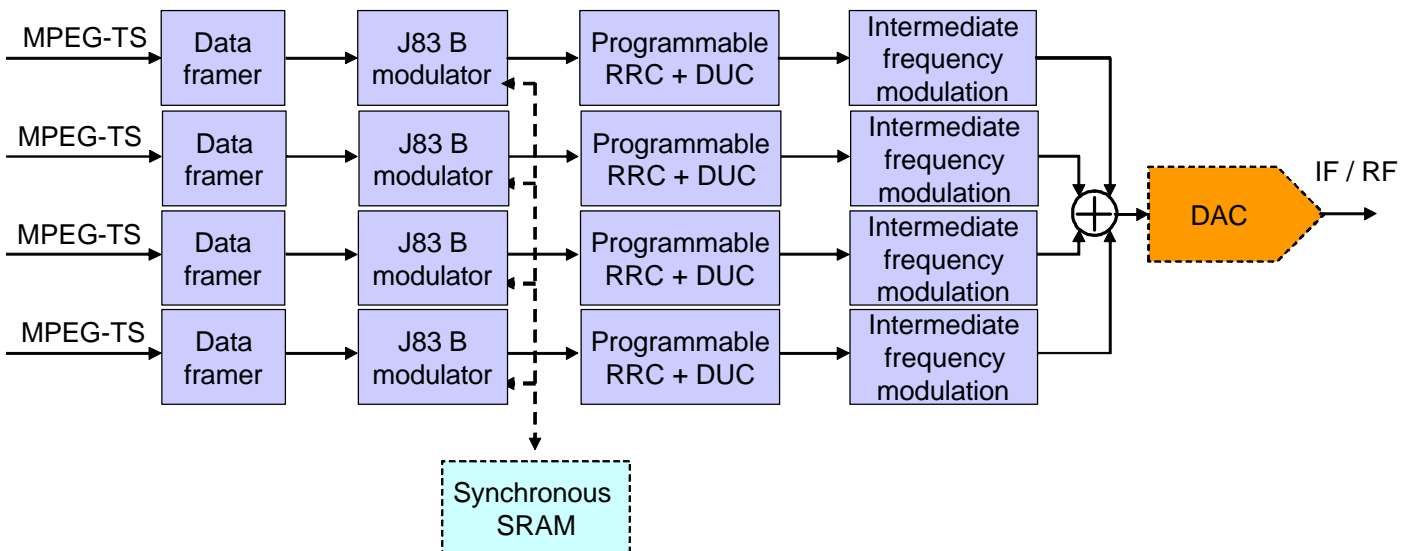
Description

The MVD cable modulator J83B core is a drop-in module that includes the following functions :

- Input data framer from DVB-SPI source (MPEG-TS flow)
- J83B modulator (Energy dispersal, Reed-Solomon encoder, interleaver, QAM symbol mapper)
- Programmable RRC filter
- Flexible Digital Up Converter
- Modulator for IF output
- Output for simple DAC (14 bits) or baseband outputs (2x16bits)

Companion cores

- Core ASI receiver
- Serial Interface for CPU configuration



Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration 4 channel with CPU and external memory interface with all interleaver modes supported.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation
Spartan 3/E/A	14 400	12	80	3	
Spartan 6	8 000	12	88	3	
Virtex 4	13 000	12	80	3	
Virtex 5	7 000	12	80	3	
Virtex 6	7 300	12	88	3	
<i>(values may vary depending on implementation options)</i>					

Ordering information and related cores

Parameters	Designation
GPIO programmable	MVD_CMDLT_J83B-4CH_GPIO_NET
CPU programmable	MVD_CMDLT_J83B-4CH_CPU_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Complementary cores : J83B 4-Channel for AD9789 DAC, Upconverter for AD9739 DAC or MAX5881 DAC, contact us.

For a multi-channel application, we recommend to use the AD9789 for 4 adjacent channels, or we recommend to use the AD9739 DAC or the MAX5881 DAC for more than 4 channels, or for non adjacent channels.

Related cores : J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer and/or ASI Receiver cores contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.