



Features

ITU-T J.83 Annex B

Compliant baseband transmitter for Cable Modem Termination Systems (CMTS)

- The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)
- Drop-in module for Virtex-6™, Virtex-5™, Spartan-6™ and Spartan™-3/E/A FPGAs
- Single clock (up to 140 MHz+ for Spartan-3/6™, 180 MHz+ for Virtex-5/6™)
- Robust SPI input (discarding incorrect input packets)
- PCR re-stamping
- Supports 5.056941 & 5.360537 symbol rates
- Programmable 64 and 256 QAM Symbol Mapping
- All interleaver modes supported thanks to external Synchronous SRAM
- Reduced interleaver modes can be implemented as internal memory
- Complex base band output (2 x 8 bits)
- Single / multi channel
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist
- MER > 43dB

Complete application fits into 3S500E and/or 3S700A depending on selected options

Applications

Cable modulator J83B may be used in applications related to cable transmission, typically at the cable head end.

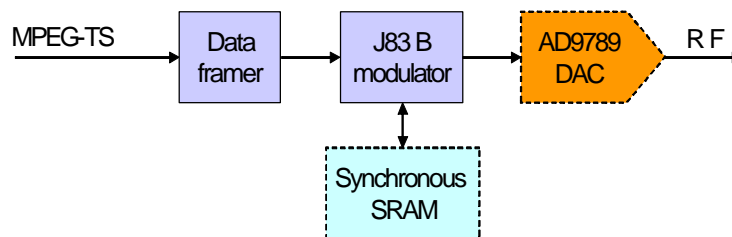
Description

The MVD cable modulator J83B core is a drop-in module that includes the following functions :

- Input data framer from DVB-SPI source (MPEG-TS flow)
- J83B modulator (Energy dispersal, Reed-Solomon encoder, interleaver, QAM symbol mapper)
- Output for complex DAC (2 x 8 bits)

Companion cores

- Core ASI receiver
- Serial Interface for CPU configuration
- I2C slave Interface core



Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU and external memory interface with all interleaver modes supported.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables : - Datasheet - Netlist for core generation
Spartan-3/E/A	1 900	3	1	3	
Spartan-6	850	2	1	3	
Virtex-5	800	2	1	3	
Virtex-6	800	2	1	3	

(values may vary depending on implementation options)

Typical configuration with CPU interface and internal memory with 8K interleaver limitation.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG
Spartan-3/E/A	1 900	10	1	2
Spartan-6	850	9	1	2
Virtex-5	800	9	1	2
Virtex-6	800	9	1	2

Typical configuration with CPU interface and internal memory with 32K interleaver limitation.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG
Spartan-3/E/A	1 900	17	1	2
Spartan-6	850	16	1	2
Virtex-5	800	16	1	2
Virtex-6	800	16	1	2

Typical configuration with CPU interface and internal memory with all interleaver modes supported.

	Slices	BRAMs (18k)	Mults/DSP48	BUFG
Spartan-3/E/A	1 900	31	1	2
Spartan-6	850	30	1	2
Virtex-5	800	30	1	2
Virtex-6	800	30	1	2

Ordering information and related cores

Parameters	Designation
GPIO programmable	MVD_CMDLT_J83B_AD9789_GPIO_NET
CPU programmable	MVD_CMDLT_J83B_AD9789_CPU_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses

Complementary cores : J83B for IF output, Upconverter for AD9739 DAC or MAX5881 DAC, contact us.
For a multi-channel application, we recommend to use the AD9789 for 4 adjacent channels, or we recommend to use the AD9739 DAC or the MAX5881 DAC for more than 4 channels, or for non adjacent channels.

Related cores : J83B 4-channel, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer and/or ASI Receiver/Transmitter cores, contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet. In addition MVD can provide on site or remote coaching.