DVB-CSA Descrambler Core V2.0

Product Brief (June 2019 - Rev B)

Description

The MVD DVB-CSA Descrambler core allows to decrypt MPEG-TS stream using ETSI specified DVB Common Scrambling Algorithm (CSA2).

Applications

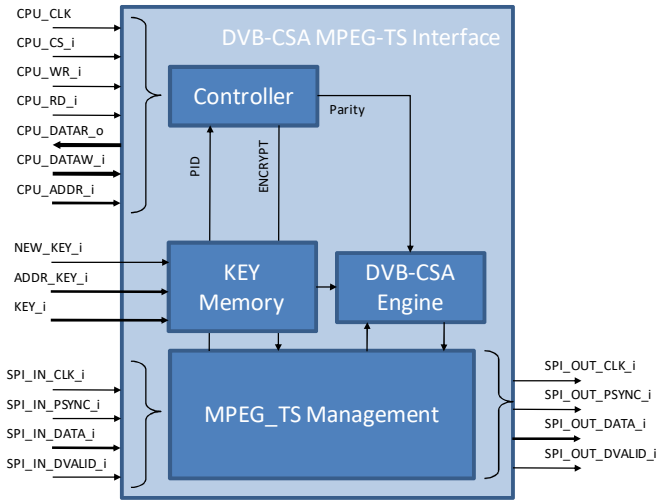
The MVD DVB-CSA Descrambler core can be used to decrypt MPEG-TS stream in order to broadcast it in a basic local network and gives access to the contents to all users.

Important note

We are only able to license these cores to customers that have signed the ETSI Non-Disclosure Agreement and are in possession of a valid license to use the Common Descrambling Algorithm.
This is a requirement on all users of this technology, applied by the consortium who own the rights to the algorithm. Please feel free to contact MVD for more information on this requirement.

Features

- **Drop-in module for Spartan™-6, Virtex™-6, Artix™-7, Kintex™-7, Virtex™-7 FPGAs and Zynq™**
- **DVB/ATSC compliant**
- **Manage automatically odd/even decryption key**
- **Selection of up to 64 PIDs and 64 Keys (32ODD/32EVEN) at the same time (any PID can use any key)**
- **Automatically removing of encryption flags of MPEG-TS packet header**
- **Supports 188, 204 and 208 bytes packet input**
- **Supports Data Packet or Data Burst format**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Resource Utilization

	Slices	LUTs	BRAMs (18k)	Mults/DSP48	BUFG
6-Series	**480**	**1340**	**1**	**0**	**1**
7-Series	**490**	**1335**	**1**	**0**	**1**

Ordering information and related cores

Designation
MVD_DVB-CSA_DESCRAMBLER_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses.

Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB-T2, DVB Remultiplexer and/or ASI interface cores, contact us.

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.