ETR101290 CORE v1.0

Product Brief (April 2022 - Rev A)

Description

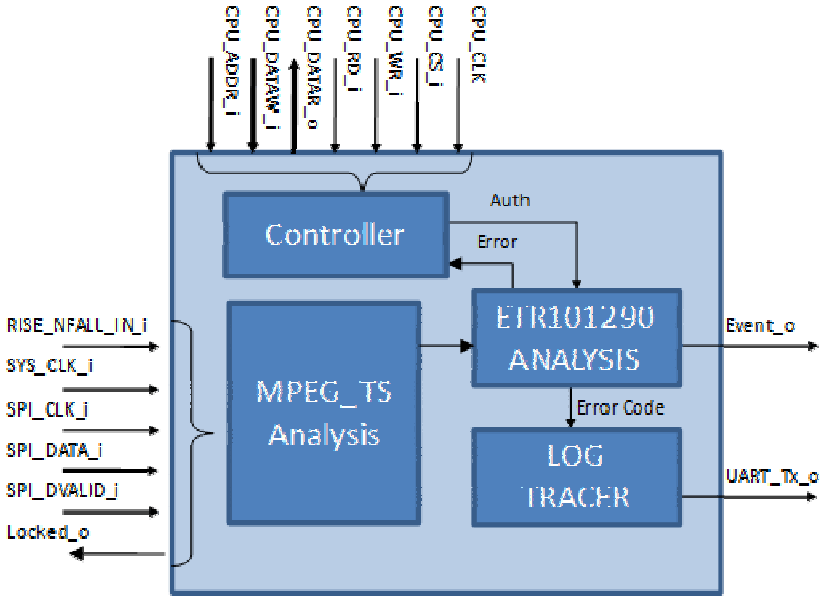
- **ETR101290 core allows to check MPEG TS stream conformity to ETSI TR 101 290 V1.4.1 (2020-06)**
- **ETR101290 is CPU programmable**
- **It includes all the processing stages to analyze PSI/SI tables and ETR101290 errors**
- **Each subpart of any priority item can be analyzed or not**
- **An output event signal can inform a CPU of a new incoming error**
- **Configurable output UART can log selected detected errors**

Applications

- **The MVD DVB ETR101290 core can be used to check the conformity of a DVB MPEG TS stream to the ETR101290 standard.**

Features

- **Drop-in module for Spartan-6™, Virtex-6™, 7 Series FPGAs and later FPGA families**
- **DVB compliant**
- **Auto adaptive and real time PSI/SI analysis**
- **Manage up to 124 services and all PID values**
- **For priority 1 (all), 2 (excepted PCR) and 3 (3.1/3.2; 3.4 to 3.6)**
- **Configurable analysis authorization**
- **Output trigger for error event**
- **Configurable UART output log**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Ordering information and related cores

Designation
MVD_ETR101290_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses
Related cores : UDP/IP stack, RX RTP, TX RTP, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at *info_cores@mvd-fpga.com*