DVB-T2 Modulator Core V1.6

Product Brief (June 2019 - Rev B)

Features

ETSI, DVB-T2 (EN 302 755 V1.1.1) compliant baseband transmitter for second generation Digital Terrestrial Television broadcasting system

- **The MVD DVB-T2 modulator core is delivered for baseband output to be natively connected to AD9789 DAC from Analog Device but can be used in Intermediate Frequency application or in RF application when respectively connected to our UPSAMPLER or our UPCONVERTER core (for Analog Devices (AD9739A) or Maxim RF DACs (MAX5881)).**
- **Drop-in module for Spartan™-6, Virtex™-6, Artix™-7, Kintex™-7, Virtex™-7, Zynq™ and above FPGAs families**
- **Dual clock (1x,2x), DAC synchronized required (up to 150 MHz for 1x Clock and for Kintex family)**
- **Robust SPI input (discarding incorrect input packets)**
- **PCR re-stamping**
- **Single PLP**
- **Single channel**

Signalization Channel :

- **Programmable BPSK, QPSK, 16-QAM and 64-QAM Symbol Mapping**
- **Guard Interval (1/2)**

Data Channel (PLP) :

- **TS data only**
- **Normal Mode or High Efficiency Mode**
- **PLP type 1 only**
- **Programmable QPSK, 16-QAM, 64-QAM and 256-QAM Symbol Mapping**
- **Constellation Rotation**
- **OFDM modes (1K, 2K, 4K, 8K, 16K, 32K)**
- **Extended Carrier mode**
- **Guard Interval (1/4, 1/8, 1/16, 1/32 - 1/128, 19/128, 19/256)**
- **Channel width from 5 MHz to 8 MHz**
- **Baseband outputs (2 x 16 bits) @ Fsymbol rate**
- **Fully synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**
- **MER > 40 dB**

Applications

The MVD DVB-T2 modulator may be used to broadcast a high rate stream (HD or 3D for example) or a multiplexed stream with many services. The standard allows choosing from a strongly robust stream to a very high data bitrate stream.

Description

The DVB-T2 core allows the transmission of an MPEG-TS data stream to a digital to analog converter in base band, IF or RF mode. The core is DVB T2 (ETSI EN 302 755 V1.1.1) compliant and support most of the standard parameters settings.

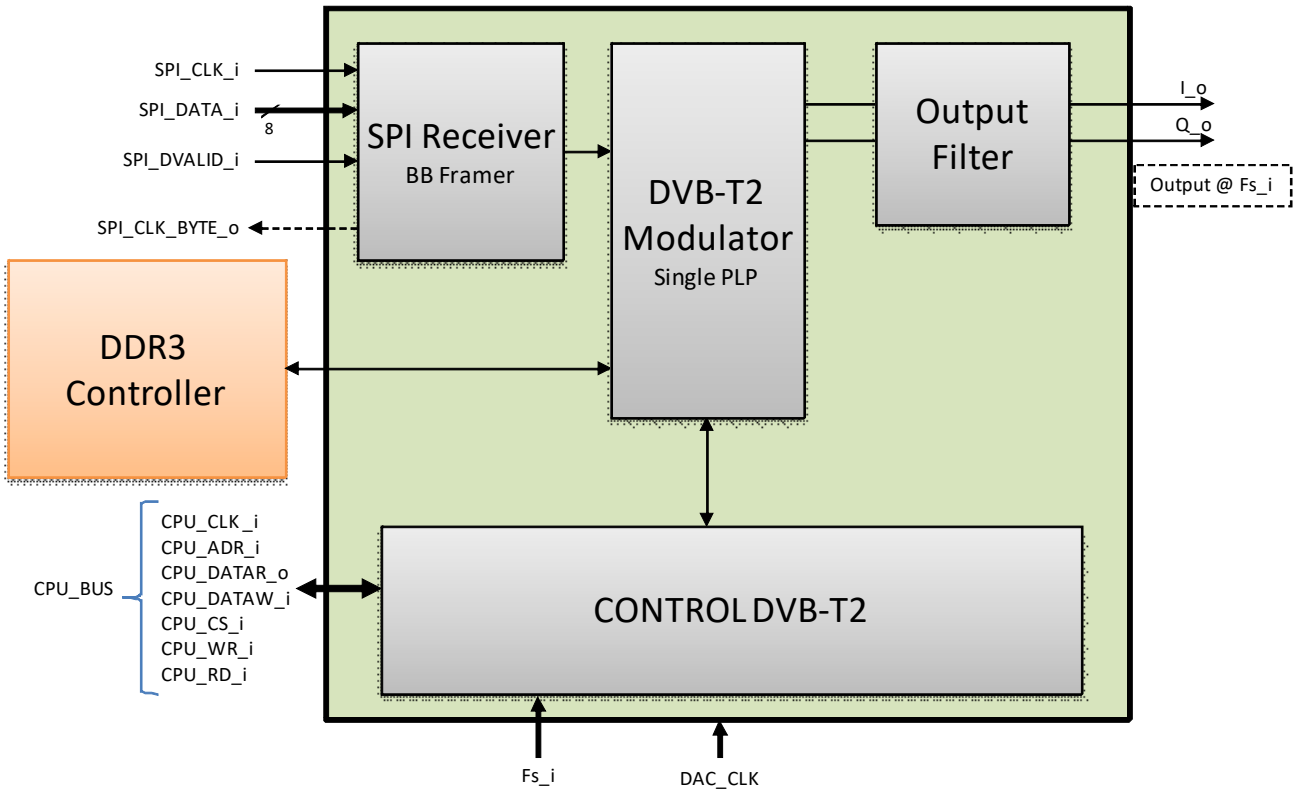
The core was developed in RTL VHDL in order to be implemented in any kind of FPGA programmable logic components. The MPEG-TS input data stream comes from a Synchronous Parallel Interface (SPI). The core output is natively designed for AD9789 but, in addition to our optional UPSAMPLER or UPCONVERTER module, can drive a simple or a complex DAC (I and Q with two 16-bit outputs) in IF or RF application. MVD delivers the core as netlist format according to targeted FPGA family.

Non supported features

- **Multiple PLP**
- **T2-MI input**
- **SFN network**
- **L1 Scrambling**
- **L1-ACE and P2 bias cells processing**
- **PAPR**
- **FEF insertion**

Companion cores

- **ASI receiver**
- **DVB remultiplexer**
- **Serial Interface for CPU configuration**
- **I2C Slave Interface**
- **Up Sampler IF**
- **Up Converter RF**



Resource Estimation

	Slices (LUT)	BRAMs (18k)	DSP48	BUFG
Spartan-6	**5000**	**102**	**45**	**2**
7 Series	**5200***	**160(*)**	**32**	**2**

*do not include required resources for 16 bit DDR3 memory controller (about 2500 slices)

MVD recommends the use of a single DDR3 1Gb : MT41J64M16

Ordering information and related cores

Parameters	Designation
Single PLP	**MVD_DVBT2_1PLP_NET**

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: Cable Modulator J83B, DVB-S, DVB-C, DVB-TH, DVB Remultiplexer and/or ASI Receiver/Transmitter cores
Contact us at *info_cores@mvd-fpga.com*

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.