Input Baseband Processing Core for Up Converter V3.0

Product Brief (February 2019 - Rev B)

Description

The Input Baseband Processing allows mixing up to 8 baseband channels.
It adds the baseband channels with full precision.
A gain register (one per channel) can adjust the output level of each baseband channel, and a saturation stage avoids the overflow.
The interval frequency between channels is dependent onthe widest bandwidth baseband input channel.
A register defines the widest bandwidth baseband input channel.

Applications

The Input Baseband Processing for Up Converter is used to mix several baseband channels to one Up Converter channel input.

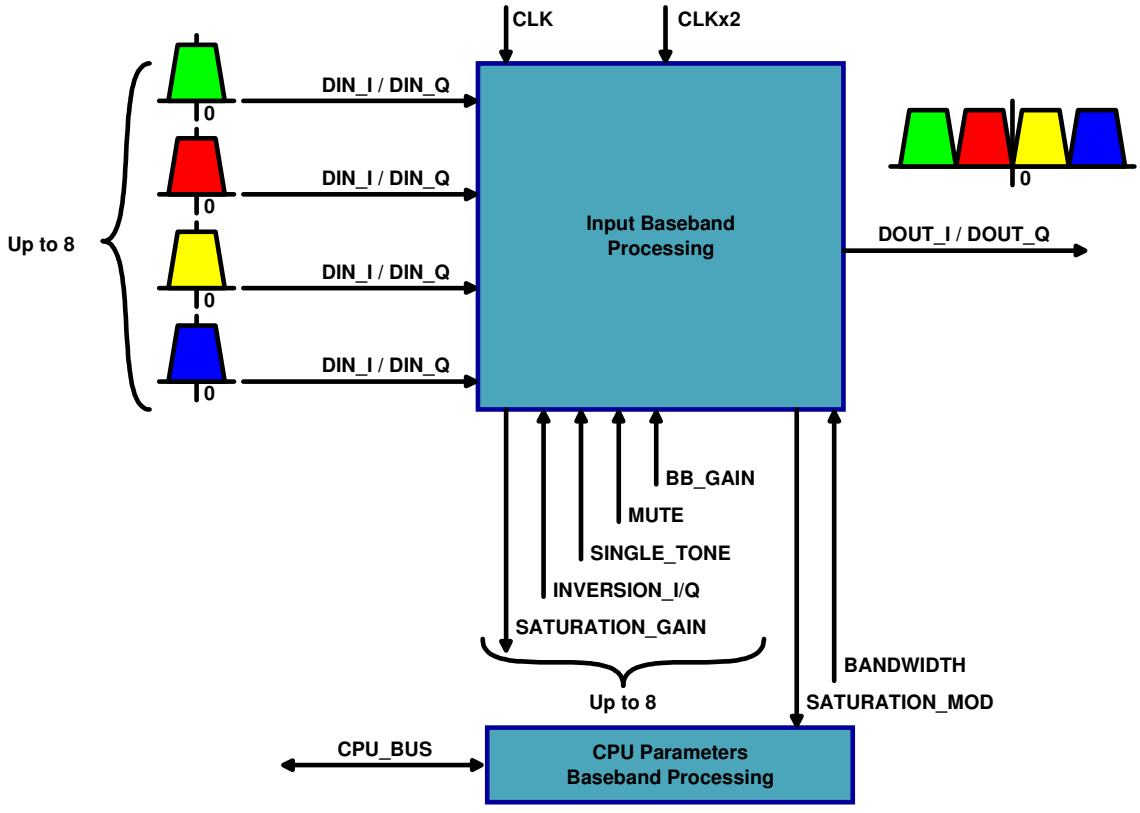
Companion cores

- **Digital RF Up Converter**
- **Output Processing**

Features

Mixes up to 8 independent baseband channels to one single channel output

- **Drop-in module for 6 Series, 7 Series and later Xilinx FPGAs**
- **Dual clocks (CLK : 125MHz or higher, CLKx2 : 250MHz or higher)**
- **Dynamically user controlled output level (individual gain for each channel)**
- **Detection of overflow for each channel (after the individual gain)**
- **Overflow prevention for each channel (after the individual gain)**
- **Possibility to invert the spectrum for each channel**
- **Mute and Single tone test on each channel**
- **Places input channels side by side at the center RF domain (0 MHz)**
- **Detection of overflow at the output (after the modulation)**
- **Overflow prevention at the output (after the modulation)**
- **Add channels with full precision**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Resource Utilization

1 channel	Slices	BRAMs 18k	DSP48
Spartan-6	**40**	**0**	**1**
7 Series	**35**	**0**	**1**

2 channels	Slices	BRAMs (18k)	DSP48
Spartan-6	**160**	**1**	**6**
7 Series	**145**	**1**	**6**

4 channels	Slices	BRAMs 18k	DSP48
Spartan-6	**330**	**2**	**12**
7 Series	**320**	**2**	**12**

8 channels	Slices	BRAMs 18k	DSP48
Spartan-6	**700**	**4**	**24**
7 Series	**680**	**4**	**24**

Ordering information and related cores

Channels count	***Designation***
1	**MVD_INPUT_BB_PROCESSING_1CH_NET**
2	**MVD_INPUT_BB_PROCESSING_2CH_NET**
4	**MVD_INPUT_BB_PROCESSING_4CH_NET**
8	**MVD_INPUT_BB_PROCESSING_8CH_NET**

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator, ATSC Remultiplexer, ASI Receiver, ASI Transmitter, Digital RF Up Converter, Interpolator x16 + RF Modulator or Output Processing cores contact us at *info_cores@mvd-fpga.com*

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.