MDIO STA Management Interface V4.0

Product Brief (February 2016 - Rev B)

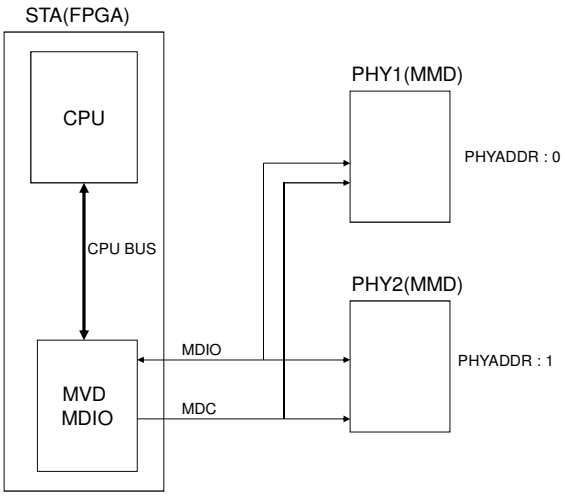
Features

MDIO Management for Ethernet PHY

- **Drop-in module for Spartan™-6, Virtex™-7, Artix™-7, Kintex™-7 and Zynq™ Xilinx FPGAs**
- **Write / Read PHY Registers**
- **MDIO Output Interface**
- **MDC clock generation**
- **Up to 32 Managed components**
- **IEEE 802.3 compliant**
- **CPU Interface for an easy control**

Description

The MVD MDIO STA Management Interface is a drop-in module for an easy control of Ethernet PHYs.



MDIO Managed System

Resource Utilization

	Slices	BRAMs	DSP48
Spartan-6	**120**	**0**	**0**
7-Series	**100**	**0**	**0**

Ordering information and related cores

Designation
MVD_MDIO_STA_INTF _NET

VHDL source code: Can be delivered as an option under NDA and other specific clauses.
Related cores: MVD UDP/IP Full Hardware Stack.
Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.

Please contact us at *info_cores@mvd-fpga.com* for more information.