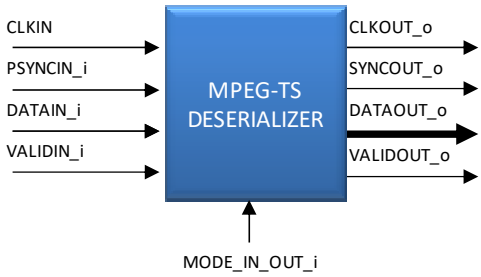
MPEG-TS_DESERIALIZER Core V2.0

Product Brief (April 2015 - Rev A)

Features

Serial MPEG_TS input stream to Parallel MPEG-TS output Stream converter

- **Drop-in module for Spartan-3™, Spartan-6™, 7-Series™ FPGAs**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**



Applications

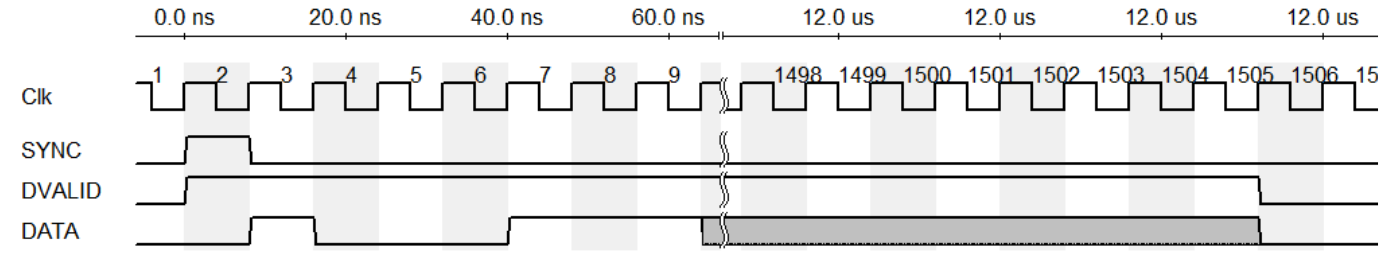
MVD MPEG-TS_DESERIALIZER may be used in applications related to DVB/MPEG transport streams for Satellite tuner data de-serialization.

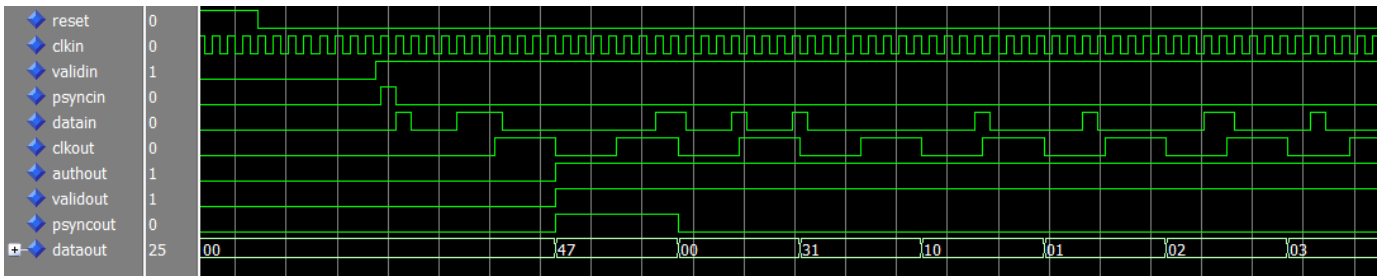
Description

The MVD MPEG-TS_DESERIALIZER core is a drop-in module that includes the following functions :

- **Data acquisition on synchronous clock (require clock capable input pin)**
- **Serial/parallel Conversion**
- **Auto adaptation to 188/204 bytes packet Input**
- **188 bytes MPEG-TS output**
- **No decoding control**
- **rising/edge input/output configurable**

Rising / falling edge are controlled by *MODE_IN_OUT_i* : bit 0 = input ; bit 1 = output. (0 = rising ; 1 = falling).





Resource Utilization The core configuration may be set by conditional synthesis .

	Slices (LUTs)	BRAMs (18k)	DSP48	CLK	Deliverables :
Spartan-3	31 (33)	0	0	1 BUFG	- Netlist for core generation
Series-6	14 (40)	0	0	1 BUFG	
Series-7	14 (38)	0	0	1 BUFIO 1 BUFR	

Ordering information and related cores

Designation
MVD_MPEG-TS_DESERIALIZER_NET

VHDL source code : can be delivered as an option under NDA and other specific clauses
Related cores : Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Transmitter cores, contact us at *info_cores@mvd-fpga.com*