



Description

The MPTS Demultiplexer core is a drop-in module that includes the following functions :

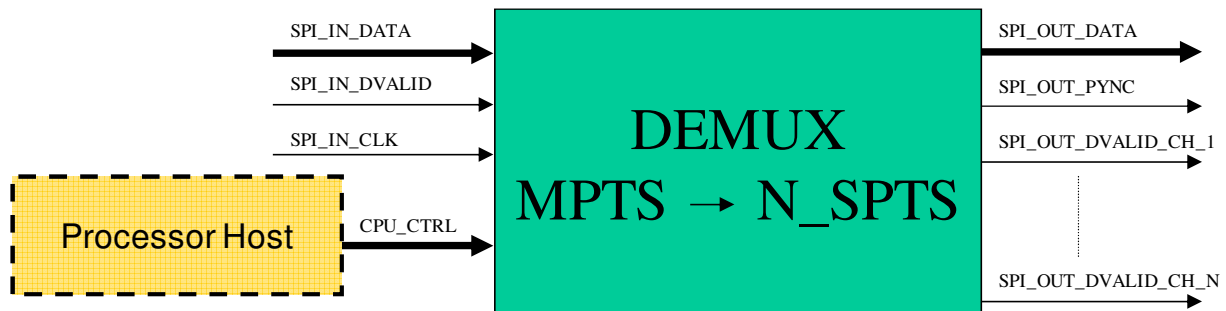
- Receives an MPTS input stream and de-multiplexes services according to the PID programming done
- De-multiplexes up to 32 services with up to 32 PIDs per service
- Automatically filters incoming tables (PAT, SDT, EIT , NIT), NULL packet and passed through PMT (if programmed) without modification, regenerate SDT and EIT for each services
- No PCR process is done as no packet is time shifted

Features

- Drop-in module for Spartan™-6, and 7-Series FPGAs
- SPI smart receiver
- CPU_interface
- Fully synthesizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist

Applications

The MPTS de-multiplexer core can be used in addition to the DVB/ATSC remultiplexer core and IPTV transmitter for SPTS to IP application.



Resource Estimation

The core configuration may be set by conditional synthesis and the FPGA resources will depend on the number of needed channels and the number of PID per channel configuration.

1 Ch. / 4-PID	Slices (LUTs)	BRAMs	Mults/DSP48
Spartan 6	498 (1085)	2	0
7 Series	574 (1057)	0	0

16 Ch. / 8-PID	Slices (LUTs)	BRAMs	Mults/DSP48
Spartan 6	773 (1562)	3	0
7 Series	743 (1535)	3	0

32 Ch. / 16-PID	Slices (LUTs)	BRAMs	Mults/DSP48
Spartan 6	992 (1963)	3	0
7 Series	875 (1964)	3	0

Ordering information and related cores

Designation
MVD_DEMUX_1_N_P_NET*

*where N (number of channel) can be from 1 to 32 and P (number of PID per channel) from 1 to 32

*By default MVD_DEMUX_1_32_16_NET is delivered, unused channel can be let opened (other configuration are delivered on request)

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP Stack, UDP/RTP Transmitter, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator. Contact us at info_cores@mvd-fpga.com

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.