Multi UDP RTP TS Receiver V1.1

Product Brief (February 2019 - Rev A)

Description

All receiver equipments which have a DVB-SPI input must be fed with a stream which respects the timing between each PCR packet.

The Multi RTP TS receiver is a module allowing to create DVB-SPI compliant stream from a UDP/(RTP) CBR Ethernet stream where MPEG-TS packets are not sent regularly (packets come in bursts) or suffer from jitter.

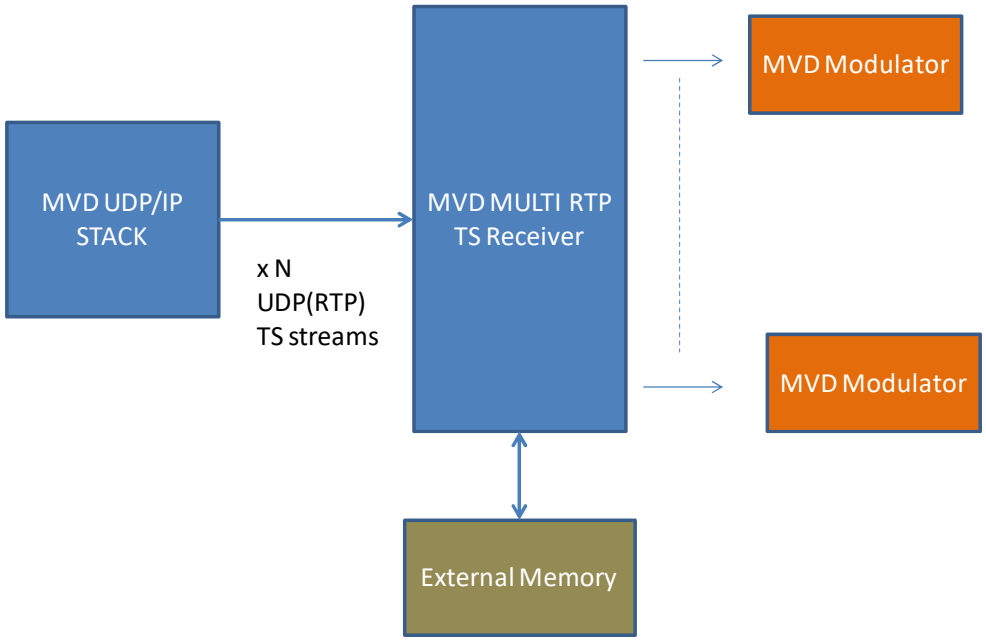
In any case, the PCR values in the incoming encapsulated stream(s) must be correct to ensure proper functioning.

Applications

The Multi RTP TS receiver can be used in applications related to IPTV reception.

Features

- **Drop-in module for Spartan™-6 and 7 Series Xilinx® FPGAs**
- **Single clock 125 MHz (same clock as Ethernet clock data)**
- **Supports up to 32 UDP(RTP) input streams**
- **Automatic detection of the input stream type (UDP only or RTP)**
- **Supports any packet length (from 1 to 7 TS, each 188 bytes length, encapsulated in UDP(RTP))**
- **DVB-SPI compliant transport stream bus output**
- **Programmable Latency for PCR mode**
- **Respects PCR Accuracy according to TR 101 290 standard (+/- 500ns) for CBR input stream**
- **BYPASS mode available for VBR input streams**
- **Auto-adjustment for a bitrate variation up to 32kbits without any discontinuity of the stream at the output**
- **For a bitrate variation higher than 32kbits, the PCR calculation is restarted**
- **CPU interface for configuration of the input streams**
- **Full synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as netlist (.ngc or .edif format)**



Resource Estimation

	Slices	BRAMs (18k)	DSP48	BUFG
Spartan-6	**200+640*N**	**4*N+1**	**2*N**	**1**
7 Series	**180+620*N**	**4*N+1**	**2*N**	**1**

where N represent the number of streams managed by the core

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Ordering information and related cores

Designation
MVD_MULTI_UDP_RTP_TS_RECEIVER_NET

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP stack, RTP Rx, RTP Tx, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator and/or ASI Receiver cores, contact us at *info_cores@mvd-fpga.com*

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.