N-SPTS to 1-MPTS Multiplexer V1.0

Product Brief (September 2019 - Rev A)

Features

- Drop-in module in charge of mixing DVB/ATSC tables and payload for SPTS stream
- Incoming stream analysis, captures ATSC/PSIP or DVB/PSI/SI sections, PMT sections and extracts needed stream parameters
- A processor interface allows to control the CORE configuration and to get basics information such as incoming bitrate, outcoming bitrate, useful payload bitrate, current FIFO state, for the general purpose part. In addition, it allows downloading PSIP/PSI/PMT tables, solving serviceID and PID conflict between inputs
- The N-SPTS to 1-MPTS Multiplexer manages the generation of output tables: new PAT, VCT, SDT, updated MGT and PMTs (when required)
- Fully synthetizable RTL VHDL design (not delivered) for easy customization
- Design delivered as Netlist

Description

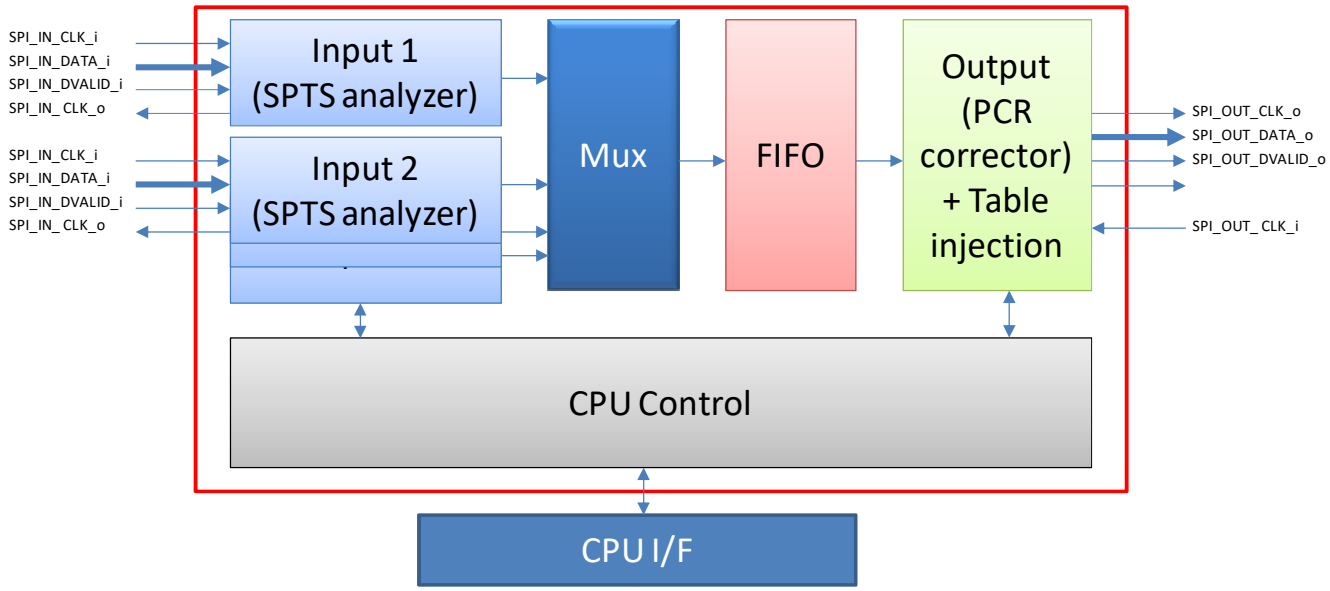
The N-SPTS to 1-MPTS Multiplexer core performs ATSC or DVB standard mixing of up to 32 incoming SPTS stream.
The input supports 188 to 255 byte frames with a maximum frequency of 13.5MHz for 108Mbits/sec.
The output is clocked from an MVD_DVBx core (in slave mode) or by itself (in master mode) with a maximum frequency of 14 MHz for 112 Mbits/sec.

The rate conversion is made through a smoothing FIFO memory (1 BRAM: up to 10 frames).

A 32-bit CPU interface is available for core control. By default the core can start up without CPU initialization; in this case, no modification is done into the stream, no conflict is managed, user must take care to incoming stream features).

Applications

N-SPTS to 1-MPTS Multiplexer may be used in applications related to transmodulation (from encoder to ATSC terrestrial channel or DVB-T terrestrial channel) or for video acquisition in case of completion of information.



Resources Estimation

Spartan-6:

Number of inputs	Slices	BRAMs (18K)	DSP48
2	1600	28	0
4	2500	37	0
8	4550	56	0
16	8400	92	0
32	15500	164	0

7 Series:

Number of inputs	Slices	BRAMs (18K)	DSP48
2	1500	28	0
4	2200	37	0
8	4250	56	0
16	8200	92	0
32	15000	164	0

Ordering information and related cores

Designation
MVD_SPTS_TO_MPTS_MUX_N_1_NET *

*where N = number of inputs

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: UDP/IP Stack, UDP/RTP Transmitter, Cable Modulator J83B, DVB-C, DVB-S, DVB-T/H, DVB Remultiplexer, ATSC modulator. Contact us at *info_cores@mvd-fpga.com*

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.