



Features

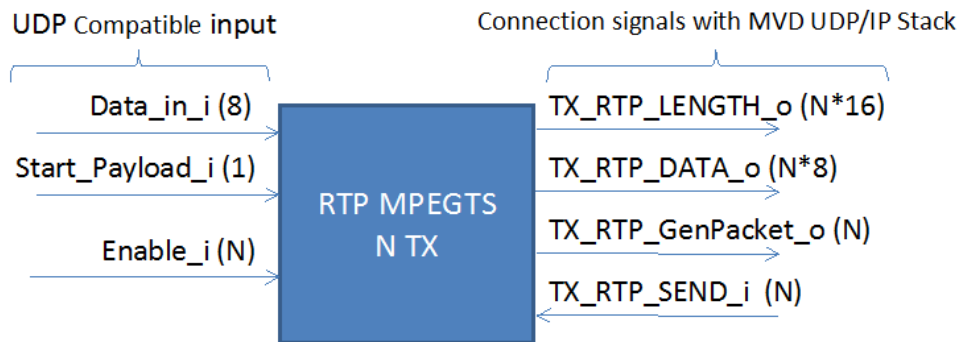
- Drop-in module for Spartan™-6/ Virtex™-6/ 7-Series Xilinx FPGAs
- Companion core of the UDP/IP Stack
- MVD UDP/IP Stack is mandatory to use this core
- RTPv2 encapsulation
- Supports only MPEG-TS payload Type
- From 1 to 7 MPEG-TS Packet per UDP / RTP Packets (configurable)
- Can support from 4 to 32 independent RTP Channels (netlist generated)
- Possibility to bypass RTP Encapsulation to perform simple UDP Encapsulation for application which requires only UDP Transmissions
- UDP compatible input
- Netlist version available for ISE 14.6 and later

Description

- The MVD Multi-RTP transmitter allows the transmission of several RTP streams on an Ethernet Network.
- MVD UDP/IP Stack is mandatory for using MVD Multi-RTP Transmitter.
- The maximum number of RTP output channels depends on FPGA resources, input bit rate and Ethernet speed connection.

Applications

MVD Multi-RTP transmitter is especially developed to transmit several MPEG-TS RTP Stream on a routed network.



Resource Estimation

The core configuration may be set by conditional synthesis and will depend on the number of needed channels and the number of PID per channel configuration.

For N Channels	Slices	BRAMs	Mults/DSP48	Deliverables :
Spartan 6 /Virtex-6 / 7-Series	80*N+30	2*N	0	- Datasheet - Netlist for core generation

Ordering information and related cores

Designation
MVD_RTP_MPEGTS_N_TX_NET

Where N can be in the interval [4,32]

When ordering the core, fives different netlists are delivered with 4,8,16,24 and 32 RTPs different channel.

If you need another number of RTP stream not in the list please contact MVD (please note that they will result in additional fees).

VHDL source code: can be delivered as an option under NDA and other specific clauses

Related cores: MVD DVB Remultiplexers, MVD Modulators, ASI receiver, MVD DVB Demux_1_N, etc. Contact us at info_cores@mvd-fpga.com

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.