UDP CPU Interface Standalone V2.0

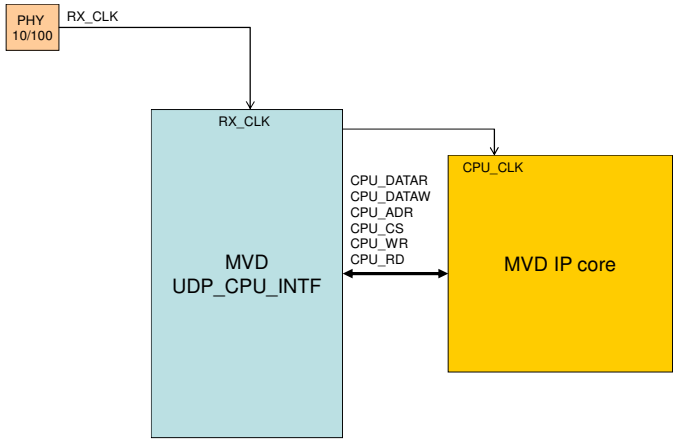
Product Brief (January 2012 - Rev A)

Features

- **Drop-in module for Spartan™-6, Virtex™-6, 7 Series Xilinx® FPGAs**
- **Companion core for all MVD IP cores**
- **Writing of main IP cores parameter settings**
- **Status reading of main IP cores**
- **Uses UDP encapsulated protocol**
- **Includes a light version of MVD UDP/IP Stack IP core**
- **Netlist version available for ISE 13 and later**

Applications

The UDP CPU Interface Standalone IP core can be used with any MVD IP cores when local CPU is not available to configure them by using Ethernet network.



Resource Utilization

	Slices	BRAMs 18K	DSP48A	BUFG	DCM
Spartan™-6	**1000**	**5**	**0**	**1**	**1**
Virtex™-6	**900**	**5**	**0**	**1**	**1**

Ordering information and related cores

Designation
UDP_CPU_INTF _STDLN_NET

VHDL source code: Can be delivered as an option under NDA and other specific clauses.

Related cores: All MVD Cores IP cores

Documentation and support: Datasheet. In addition MVD can provide on site or remote coaching.

Please contact us at *info_cores@mvd-fpga.com* for more information.