



Features

- ITU-T J.83 Annex B, Compliant baseband transmitter for Cable Modem Termination Systems (CMTS)
- Drop-in module for Virtex-5™, Virtex-4™ and Spartan™-3/E/A FPGAs
 - Supports all interleaved modes
 - Supports 5.056941 & 5.360537 symbol rates
 - PCR restamping
 - Single channel – support for multi channel
 - Single clock (up to 140 MHz+ for Spartan-3™, 180 MHz+ for Virtex-4™ and Virtex-5™)
 - Programmable 64 and 256 QAM Symbol Mapping
 - Full synthetizable RTL VHDL design (not delivered) for easy customization
 - Netlist version available for ISE 9.2 and later versions
 - MER > 43dB
 - Controller for ZBT memory (controller for internal BRAM in option)

Applications

May be used in applications related to cable transmission, typically at the cable head end.

Description

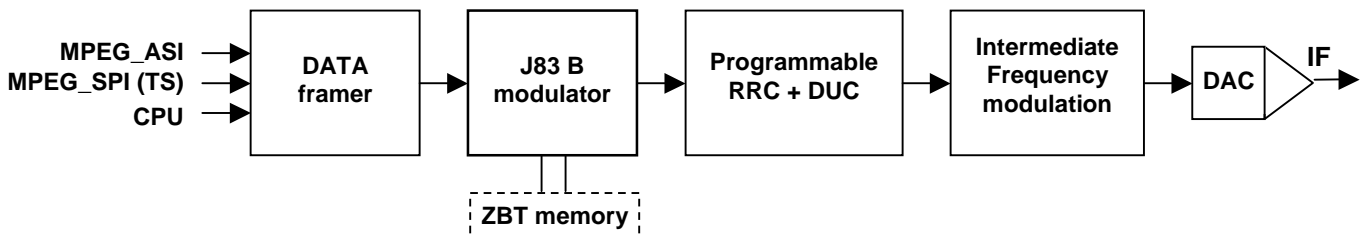
The MVD Cable modulator J83B core is a drop-in module that includes the following functions :

- Input data framer from Microprocessor, MPEG_ASI or MPEG_SPI source (MPEG_TS flow)
- J83B modulator (Energy dispersal, Reed Solomon encoder, QAM symbol mapper)
- Programmable RRC filter
- Flexible Digital Up Converter
- Modulator for FI output
- Output for simple DAC (14 bits) or complex DAC (2x16bits)

The MVD Cable modulator J83B core can be customized for specific application. In option, it can include :

- ASI interface core
- Direct 32 bit CPU interface for configuration parameters and MPEG_TS input flow
- Controller for internal BRAM

Complete application fits into 3S500E and/or 3S700A depending on selected options.



Resource Utilization The core configuration may be set by conditional synthesis . Typical configuration with SPI (MPEG TS) input and CPU interface.

	Slices	BRAMs	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation and testbench for simulation
Spartan3/E/A	4 600	13	20	3	
Virtex 4	4 200	12	31	3	
Virtex 5	2 500	8	31	3	

(values may vary depending on implementation options)



Ordering information and related cores

Parameters	Interfaces for MPEG_TS input stream	Designation
Fixed	SPI	MVD_CMDLT_J83B_FIXED_SPI_NET
Fixed	ASI (1)	MVD_CMDLT_J83B_FIXED_ASI_NET
GPIO programmable	SPI	MVD_CMDLT_J83B_GPIO_SPI_NET
GPIO programmable	ASI (1)	MVD_CMDLT_J83B_GPIO_ASI_NET
CPU programmable	SPI	MVD_CMDLT_J83B_CPU_SPI_NET
CPU programmable	SPI + ASI (1) +CPU (2)	MVD_CMDLT_J83B_CPU_SPI_ASI_CPU_NET
4 channels	SPI + CPU (2)	MVD_CMDLT_J83B_CPU_SPI_M_NET

Related cores : DVB-C for J83A/C, DVB-S, DVB-T/H and Remultiplexer,
contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.



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