



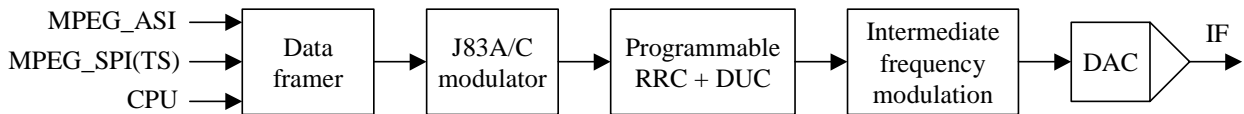
Features

ITU-T J.83 Annex A/C, DVB-C (ETS 300 429)
Compliant baseband transmitter for Cable Modem Termination Systems (CMTS)

- Drop-in module for Virtex-5™, Virtex-4™ and Spartan™-3/E/A FPGAs
- Supports programmable symbol rates
- PCR restamping
- Single channel – support for multi channel
- Single clock (up to 140 MHz+ for Spartan-3™, 180 MHz+ for Virtex-4™ and Virtex-5™)
- Programmable 16, 32, 64, 128 and 256 QAM Symbol Mapping
- Full synthesizable RTL VHDL design (not delivered) for easy customization
- Netlist version available for ISE 9.2 and later versions
- MER > 43dB

Applications

DVB-C may be used in applications related to cable transmission, typically at the cable head end.



Description

The MVD DVB-C core is a drop-in module that includes the following functions :

- Input data framer from Microprocessor, MPEG_ASI or MPEG_SPI source (MPEG_TS flow)
- J83AC modulator (Energy dispersal, Reed Solomon encoder, interleaver, QAM symbol mapper)
- Programmable RRC filter for annex A and C
- Flexible Digital Up Converter
- Modulator for IF output
- Output for simple DAC (14 bits) or complex DAC (2x16bits)

The MVD DVB-C core can be customized for specific application. In option, it can include :

- ASI interface core
- Ethernet UDP core for video on IP
- Direct 32 bit CPU interface for configuration parameters and MPEG_TS input flow

Complete application fits into 3S500E and/or 3S700A depending on selected options.

Resource Utilization The core configuration may be set by conditional synthesis . Typical configuration with SPI (MPEG TS) input , CPU interface and simple DAC output.

	Slices	BRAMs	Mults/DSP48	BUFG	Deliverables : Datasheet and user's guide Netlist for core generation and testbench for simulation
Spartan3/E/A	4 500	6	20	2	
Virtex 4	3 400	6	24	2	
Virtex 5	1 500	4	24	2	

(values may vary depending on implementation options)

Ordering information and related cores

Parameters	Interfaces for MPEG_TS input stream	Designation
Fixed	SPI	MVD_DVBC_J83AC_FIXED_SPI_NET
Fixed	ASI (1)	MVD_DVBC_J83AC_FIXED_ASI_NET
GPIO programmable	SPI	MVD_DVBC_J83AC_GPIO_SPI_NET
GPIO programmable	ASI (1)	MVD_DVBC_J83AC_GPIO_ASI_NET
CPU programmable	SPI	MVD_DVBC_J83AC_CPU_SPI_NET
CPU programmable	SPI + ASI (1) +CPU (2)	MVD_DVBC_J83AC_CPU_SPI_ASI_CPU_NET

(1) ASI can be serial or parallel (please specify).

(2) CPU interfaces compatible with 8, 16 or 32-bit, big or little endian processors.

VHDL source code : can be delivered as an option under NDA and other specific clauses

Related cores : Cable Modulator J83B, DVB-S and/or DVB-T/H cores contact us at info_cores@mvd-fpga.com

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.

