



**Features**

Reception side Udp / Ip / Mac stack, a real time UDP offload engine

- Drop-in module for Virtex-5™, Virtex-4™
- Programmable filter for broadcast
- Programmable filter for IP source/destination address
- Programmable filter for UDP destination port
- Different fields available in registers
- Support JUMBO frame in option
- Clock up to 125 MHz for Virtex-4/5™
- Netlist version available for ISE 8.2 and later

**Description**

The MVD “UDP Receive engine” core is a drop-in module that includes the following functions :

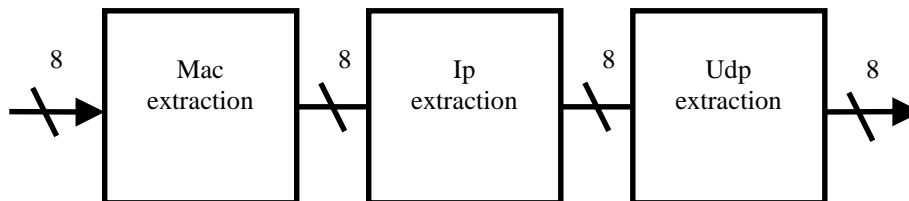
- Full hardware UDP extraction
  - Full hardware IP extraction
  - Different programmable filters on protocol fields
  - IP fragmentation not supported
  - Directly connectable with the XILINX TEMAC
  - Programmable with a Microblaze or a PPC405
- Up to 450 Mbits/sec

Design up to 125 MHz for Virtex-4/5™.

**Applications**

MVD Hw UDP stack may be used in applications related to Ethernet reception, especially with XILINX FPGA technology

MVD can also provide additional remote or on-site support or cores for UDP Tx, ARP, ICMP, DHCP ...



**Resource Utilization**

	Slices	BRAMs	BUFG	Deliverables Netlist for core generation and simulation : ISE 8.2, 9.1, 9.2
Virtex 4	400	2	1	
Virtex 5	360	1	1	

**Ordering information and related cores**

Netlist version : MVD\_UDPRX\_NET\_8.2  
 Netlist version : MVD\_UDPRX\_NET\_9.1  
 Netlist version : MVD\_UDPRX\_NET\_9.2

Related cores : UDP Transmit engine, ARP hardware module, MPEG-TS framer, ... (VHDL or netlist versions) contact us

