ARM-7 / ARM-9 HARDWARE DESIGN

Ref : 002579A **Duration : 4 days**

OBJECTIVES

- This course takes an **in depth** look at the considerations you will need to take into account when designing a system containing an ARM-7/ARM-9 core. Information on the latest generation of ARM processor cores, is also included.
- It is aimed at hardware engineers who need to understand how to design ARM based systems, but also wish to obtain minimum understanding of the issues of writing software to run on that system
- The AMBA busses are viewed in detail
- ARM debug solutions are explained

RELATED COURSES

- ARM-7 / ARM-9 System Design (Ref.002879A)

PARTNERS

- This training course is approved by ARM

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential
- A basic awareness ARM cores is useful but not essential

APPROVED TRAINING CENTRE ARM

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

First day

THE ARM ARCHITECTURE

- Overview of ARM
- Registers
- Modes
- Exception handling
- Instruction sets

ARM CPU ARCHITECTURE

- ARM7TDMI and ARM9TDMI pipelines
- Datapaths
- Instruction decoding
- Overview of ARM9E-S, StrongARM and Xscale

MEMORY

- Caches
- Write buffers
- Tightly Coupled Memories
- Configuration & Control
- Memory Protection Unit
- Memory Management Unit
- Endian Configuration
- Data Alignment

ARM INSTRUCTION SETS

- ARM v4T
- Conditional Execution
- Data processing Instructions
- Branch Instructions
- Status Register Instructions
- Load & Store Instructions
- Coprocessor Instructions
- Exception Generating Instructions
- ARM v5TE(J)
- Conditional Execution
- Data processing Instructions
- Branch Instructions
- Status Register Instructions
- Load & Store Instructions
- Coprocessor Instructions
- Exception Generating Instructions
- Thumb

EXCEPTION HANDLING

- Exception priority
- Vector table instructions
- Chaining exception handlers
- Register usage in exception handlers
- Example C interrupt handler
- Software managed interrupt controller
- Issues when reenabling interrupts
- Invoking SWIs
- Data abort with memory management

Second day

AMBA3.0 INTERCONNECT SPECIFICATION

- Purpose of this specification
- Example of SoC based on AMBA specification
- Differences between AMBA2.0 and AMBA3.0

AHB - ADVANCED HIGH PERFORMANCE BUS

- Centralized address decoding
- Address gating logic
- Arbitration, bus parking
- Single-data transactions
- Sequential transfers
- Retry response
- Split response
- AHB-lite specification

APB - ADVANCED PERIPHERAL BUS

- Read timing diagram
- Write timing diagram
- Operation of the AHB-to-APB bridge
- APB3.0 new features

Third day

ARM7TDMI

- Processor
- Memory Interface

ARM946E

- Processor
- Interfaces
- Implementation

ARM946/966 COPROCESSORS

- ARM922T
- Processor
- Memory Management

Fourth day

DEBUGGING ARM-BASED SYSTEMS

- Introduction
- Breakpoints and Watchpoints
- Debug State
- Debug Communications Channel
- Application Debug
- Designing for Debug

TRACING ARM-BASED SYSTEMS

- Introduction
- Embedded Trace Macrocell
- Embedded Trace Buffer
- TPA & Trace Software

ARM PROCESSOR INTEGRATION

- Functional Integration
- DFT Integration
- Functional Verification
- DFT Verification
- Synthesis
- Physical Integration
- Post-Layout Verification

DOCUMENTATION

Training manuals will be given to attendees during training in print.